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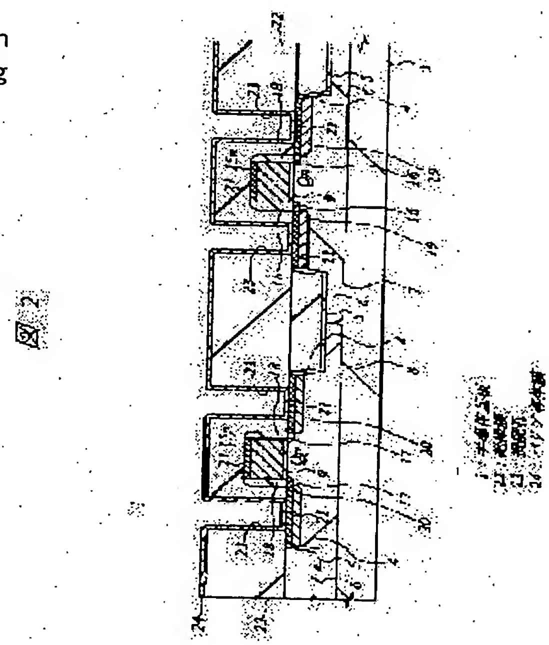
(54) METHOD FOR FABRICATING SEMICONDUCTOR INTEGRATED CIRCUIT

(57)Abstract:
PROBLEM TO BE SOLVED: To protect a gate oxide film against breakdown due to charge up damage by reducing inflow of plasma electrons, generated at the time of depositing a thin film by sputtering, to a semiconductor substrate.
SOLUTION: In a process for making contact holes 23 in an insulation film 22 and depositing a barrier conductor film 24 on the surface of the insulation film 22 including the inside of the contact holes 23 by sputtering, means for reducing inflow of plasma electrons to a semiconductor substrate 1 is employed for depositing the barrier conductor film 24. As the means for reducing inflow of plasma electrons to the semiconductor substrate 1, a collimation sputtering system or a long throw sputtering system is employed.



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CLAIMS

[Claim(s)]
[Claim 1] It is the manufacture approach of the semiconductor integrated circuit equipment which includes the 1st and 2nd sputtering processes in order, and is characterized by said 1st sputtering process being the sputtering method which controls the inflow to said semi-conductor substrate of the electron generated in sputtering in case the conductive film is deposited on the front face of the insulator layer deposited on the principal plane of a semi-conductor substrate after puncturing a connection hole.
[Claim 2] (a) the process which deposits the 1st conductivity film on the front face of the insulator layer which deposited on the principal plane of a semi-conductor substrate by the sputtering method after puncturing a connection hole, and (b) -- the manufacture approach of the semiconductor integrated circuit equipment characterized by to deposit said 1st conductivity film on the sputtering conditions which control the inflow to said semi-conductor substrate of the electron generated in sputtering including the process which deposits the 2nd conductivity film on the front face of said 1st conductivity film.
[Claim 3] (a) After puncturing a connection hole on the front face of the insulator layer deposited on the principal plane of a semi-conductor substrate, The process which deposits the 1st conductivity film by the sputtering method, the process which deposits the 2nd conductivity film on the front face of the 1st conductivity film of (b) above, An implication and said 1st conductivity film The collimation sputtering method, The manufacture approach of the semiconductor integrated circuit equipment characterized by depositing by the sputtering method which made it the discharge-gas-pressure force conditions controlled or prevented for the electron generated in the long slow sputtering method or sputtering to flow into said semi-conductor substrate.
[Claim 4] (a) It is the manufacture approach of the semiconductor integrated circuit equipment which includes the 1st and 2nd sputtering processes in order, and is characterized by for said 1st sputtering process to be the sputtering method which controls the inflow to said semi-conductor substrate of the electron generated in sputtering in case the conductive film is deposited on the front face of said insulator layer containing said plug after forming a plug in the insulator layer deposited on the principal plane of a semi-conductor substrate.
[Claim 5] (a) After forming a plug in the insulator layer deposited on the principal plane of a semi-conductor substrate, The process which deposits the 1st conductivity film on the front face of said insulator layer containing said plug by the sputtering method, (b) Said 1st conductivity film is the manufacture approach of the semiconductor integrated circuit equipment characterized by depositing on the sputtering conditions which control the inflow to said semi-conductor substrate of the electron generated in sputtering including the process which deposits the 2nd conductivity film on the front face of said 1st conductivity film.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] About the manufacturing technology of semiconductor integrated circuit equipment, by the sputtering method which used the plasma, especially this invention is applied to the manufacturing technology of the semiconductor integrated circuit equipment which a thin film deposits, and relates to an effective technique.
[0002]
[Description of the Prior Art] In the thin film formation process of semiconductor integrated circuit equipment of having MISFET (Metal Insulator Semiconductor Field Effect Transistor), as for most about the membrane formation performed by the sputtering method, the magnetron sputtering method has been used for improvement in the speed of thin film formation, for example as indicated by November 22, 1991, "1992 Edition VLSI manufacture and a testing-device guidebook" of Kogyo Chosakai Publishing Issue, and p84-p93.
[0003] Since the current magnetron sputtering method has the thing of the system which the plasma can generate and form with mainly comparatively low gas pressure in use and the (a) low battery and the ideal discharge property of a high current are acquired Since the atom by which (b) spatter whose sputtering effectiveness per power consumption improves is carried out reaches efficiently the semi-conductor substrate countered and arranged Since the collision of the electron to (c) semi-conductor substrate in which membrane formation at a high speed is possible can be reduced, the rise of the temperature of a semi-conductor substrate is reduced and it has the description of ** in which membrane formation at low temperature is possible.
[0004]
[Problem(s) to be Solved by the Invention] However, this invention persons found out producing the following problems in the Prior art which deposits a thin film by the magnetron sputtering method for using plasma equipment.
[0005] That is, the electron in the plasma flows on a semi-conductor substrate so that the magnetic field of a magnet may be met. This electron that flowed is accumulated in a semi-conductor substrate, and the potential difference arises in the part into which the electron of a semi-conductor substrate flows, and other parts. When the current (damage current) resulting from this potential difference flows a semi-conductor substrate, the gate oxide of MISFET formed on the principal plane of a semi-conductor substrate may break or deteriorate. Therefore, it is necessary to cope with the sputtering system which uses the plasma and to use the spatter chamber and process which check the inflow to an electronic semi-conductor substrate.
[0006] The purpose of this invention is to offer the technique which deposits a thin film by the sputtering method using the plasma, without destroying or deteriorating the gate oxide of MISFET.
[0007] The other purposes and the new description will become clear from description and the accompanying drawing of this specification along [said] this invention.

explained among invention indicated in this application.
[0009] That is, in case this invention deposits the conductive film on the front face of the insulator layer deposited on the principal plane of a semi-conductor substrate after puncturing a connection hole, the 1st and 2nd sputtering processes are included in order, and said 1st sputtering process is the sputtering method which controls the inflow to said semi-conductor substrate of the electron generated in sputtering.
[0010] Moreover, said 1st conductivity film deposits including the process which deposits the 1st conductivity film by the sputtering method, and the process which deposits the 2nd conductivity film used as the main conductive layer on the front face of said 1st conductivity film on the sputtering conditions which control the inflow to said semi-conductor substrate of the electron generated in sputtering after this invention's puncturing a connection hole on the front face of the insulator layer deposited on the principal plane of a semi-conductor substrate.
[0011] Moreover, said 1st conductivity film is deposited by the collimation sputtering method including the process which deposits the 1st conductivity film by the sputtering method, and the process which deposits the 2nd conductivity film used as the main conductive layer on the front face of said 1st conductivity film after this invention's puncturing a connection hole on the front face of the insulator layer deposited on the principal plane of a semi-conductor substrate.
[0012] Moreover, said 1st conductivity film is deposited by the long slow sputtering method including the process which deposits the 1st conductivity film by the sputtering method, and the process which deposits the 2nd conductivity film used as the main conductive layer on the front face of said 1st conductivity film after this invention's puncturing a connection hole on the front face of the insulator layer deposited on the principal plane of a semi-conductor substrate.
[0013] Moreover, the process which deposits the 1st conductivity film by the sputtering method after this invention's puncturing a connection hole on the front face of the insulator layer deposited on the principal plane of a semi-conductor substrate, It is a thing including the process which deposits the 2nd conductivity film used as the main conductive layer on the front face of said 1st conductivity film. Said 1st conductivity film In order to prevent the electron generated in sputtering flowing into said semi-conductor substrate, it deposits by the sputtering method of the discharge-gas-pressure force of colliding with argon gas at least 4 times or more by the time a plasma electron reaches a semi-conductor substrate.
[0014] Moreover, said 1st conductivity film is deposited including the process which deposits the 1st conductivity film by the sputtering method, and the process which deposits the 2nd conductivity film used as the main conductive layer on the front face of said 1st conductivity film by the sputtering method under the conditions which made temperature of said semi-conductor substrate 100 degrees C or less after this invention's puncturing a connection hole on the front face of the insulator layer deposited on the principal plane of a semi-conductor substrate.
[0015] Moreover, in case this invention deposits the conductive film on the front face of said insulator layer containing said plug after forming a plug in the insulator layer deposited on the principal plane of a semi-conductor substrate, it includes the 1st and 2nd sputtering processes in order, and said 1st sputtering process is the sputtering method which controls the inflow to said semi-conductor substrate of the electron generated in sputtering.
[0016] Moreover, the process which deposits the 1st conductivity film on the front face of said insulator layer containing said plug by the sputtering method after this invention forms a plug in the insulator layer deposited on the principal plane of a semi-conductor substrate, Said 1st conductivity film is deposited including the process which deposits the 2nd conductivity film used as the main conductive layer on the front face of said 1st conductivity film on the sputtering conditions which control the inflow to said semi-conductor substrate of the electron generated in sputtering.
[0017] Since it can prevent the plasma electron generated at the time of sputtering flowing into a gate electrode through a connection hole in case the conductive film is deposited at the 1st sputtering process on the insulator layer containing a connection hole according to above-mentioned this invention, it can prevent the potential difference arising in the part into which the electron of a semi-conductor substrate flows, and other parts. Consequently, since the current

(charge-up damage current) resulting from said potential difference can prevent flowing said semi-conductor substrate, the destruction or degradation of the gate oxide of MISFET formed on the principal plane of said semi-conductor substrate can be prevented, and the yield and dependability of semiconductor integrated circuit equipment can be raised.

[0018] Moreover, even said semi-conductor substrate can make it hard to reach a plasma electron on the insulator layer containing a connection hole by making the 1st conductivity film into the discharge-gas-pressure force of colliding the sputtering method with an argon atom at least 4 times or more by the time a plasma electron reaches a semi-conductor substrate in case it uses and deposits according to above-mentioned this invention. Consequently, since it can prevent a plasma electron flowing into a gate electrode through a connection hole, the destruction or degradation of the gate oxide of MISFET resulting from a charge-up damage current flowing can be prevented, and the yield and dependability of semiconductor integrated circuit equipment can be raised.

[0019] Moreover, according to above-mentioned this invention, the amount value of charges since the sputtering method is used and deposited, in case the gate oxide of MISFET destroys the 1st conductivity film on the insulator layer which contains a connection hole under the conditions which made temperature of a semi-conductor substrate 100 degrees C or less can be improved. Consequently, the destruction or degradation of said gate oxide resulting from a charge-up damage current can be prevented, and the yield and dependability of semiconductor integrated circuit equipment can be raised.

[0020]

[Embodiment of the Invention] Hereafter, the gestalt of operation of this invention is explained to a detail based on a drawing. In addition, in the complete diagram for explaining the gestalt of operation, the same sign is given to the member which has the same function, and explanation of the repeat is omitted.

[0021] (Gestalt 1 of operation) The gestalt 1 of this operation applies this invention to the manufacture approach of the semiconductor integrated circuit equipment constituted from an n channel mold MISFETQn and a p channel mold MISFETQp.

[0022] Hereafter, the manufacture approach of the above-mentioned semiconductor integrated circuit equipment is explained in order of a process using drawing 1 - drawing 9 .

[0023] First, as shown in drawing 1 , the semi-conductor substrate 1 which consists of single crystal silicon whose specific resistance is about 10ohmcm is heat-treated at about 850 degrees C. The thin silicon oxide film (pad oxide film) of about 10nm of thickness is formed in the principal plane. subsequently, this silicon oxide film top -- the silicon nitride film of about 120nm of thickness -- CVD (Chemical Vapor Deposition), after depositing in law The silicon nitride film and silicon oxide film of a component isolation region are removed by the dry etching which used the photoresist film as the mask. When densifying the silicon oxide film embedded to the interior of an isolation slot at a next process (biscuit ware), the silicon oxide film is formed in order to ease the stress which joins a substrate. Moreover, since a silicon nitride film has the property which cannot oxidize easily, it is used as a mask which prevents oxidation on the front face of a substrate of the lower part (active region).

[0024] Then, after forming a slot with a depth of about 350nm in the semi-conductor substrate 1 of a component isolation region by the dry etching which used the silicon nitride film as the mask, in order to remove the damage layer produced in the wall of a slot by etching, the semi-conductor substrate 1 is heat-treated at about 1000 degrees C, and the thin silicon oxide film 5 of about 10nm of thickness is formed in the wall of a slot.

[0025] Then, in order to deposit the silicon oxide film 6 of about 380nm of thickness with a CVD method on the semi-conductor substrate 1 and to improve the membraneous quality of the silicon oxide film 6 subsequently, the semi-conductor substrate 1 is heat-treated and the silicon oxide film 6 is densified (eye thermal shrinking). then, chemical mechanical polishing (Chemical Mechanical Polishing;CMP) which used the silicon nitride film for the stopper -- a front face forms the isolation slot 4 by which flattening was carried out by grinding the silicon oxide film 6 by law, and leaving the interior of a slot.

[0026] then, the field which forms the n channel mold MISFET of the semi-conductor substrate

1 after removing the silicon nitride film which remained on the active region of the semi-conductor substrate 1 by the wet etching using a heat phosphoric acid -- B (boron) -- an ion implantation -- carrying out -- p mold -- the field which forms a well 7 and forms the p channel mold MISFET -- P (Lynn) -- an ion implantation -- carrying out -- n mold -- a well 8 is formed.
[0027] then, p mold -- a well 7 and n mold -- the semi-conductor substrate 1 after removing the silicon oxide film of each front face of a well 8 using the penetrant remover of HF (fluoric acid) system -- wet oxidation -- carrying out -- p mold -- a well 7 and n mold -- pure gate oxide 9 of about 3.5nm of thickness is formed in each front face of a well 8.
[0028] Next, the non dope polycrystalline silicon film of about 90-100nm of thickness is deposited with a CVD method on the semi-conductor substrate 1. Then, using the mask of an ion notes necessity, the ion implantation of the P (Lynn) is carried out to the non dope polycrystalline silicon film of the upper part of a well 7 p molds, and n mold polycrystalline silicon film is formed. Furthermore it continues, the ion implantation of the B (boron) is carried out to the non dope polycrystalline silicon film of a well 8 n molds using the mask of an ion notes necessity, and p mold polycrystalline silicon film is formed.
[0029] Next, the photoresist film is used as a mask and dry etching of n mold polycrystalline silicon film and the p mold polycrystalline silicon film is carried out. 15n of gate electrodes of the n channel mold MISFET which consists of n mold polycrystalline silicon is formed in the upper part of the gate oxide 9 of a well 7 p molds by this, and gate electrode 15p of the p channel mold MISFET which consists of p mold polycrystalline silicon film is formed in the upper part of the gate oxide 9 of a well 8 n molds. The gate length of 15n of gate electrodes and gate electrode 15p is 0.25 micrometers.
[0030] Next, after removing the photoresist film used for processing of the gate electrodes 15n and 15p, n-mold semiconductor region 16 is formed in a well 7. p mold -- a well 7 -- n mold impurity (Lynn), for example, P, -- an ion implantation -- carrying out -- p mold of the both sides of 15n of gate electrodes -- n mold -- a well 8 -- p mold impurity (boron), for example, B, -- an ion implantation -- carrying out -- n mold of the both sides of gate electrode 15p -- p-mold semiconductor region 17 is formed in a well 8.
[0031] next, the semi-conductor substrate 1 top -- the silicon oxide film of about 100nm of thickness -- a CVD method -- depositing -- reactive ion etching (RIE) -- the sidewall spacer 18 is formed in 15n of gate electrodes of the n channel mold MISFET, and each side attachment wall of gate electrode 15p of the p channel mold MISFET by carrying out anisotropic etching of this silicon oxide film using law. then, p mold -- a well 7 -- n mold impurity (arsenic), for example, As, -- an ion implantation -- carrying out -- n+ mold semiconductor region 19 (the source, drain) of the n channel mold MISFET -- forming -- n mold -- the ion implantation of p mold impurity (boron), for example, the B, is carried out to a well 8, and p+ mold semiconductor region 20 (the source, drain) of the p channel mold MISFET is formed. Thereby, the source of LDD (Lightly Doped Drain) structure and a drain field are formed in each of the n channel mold MISFET and the p channel mold MISFET, and the n channel mold MISFETQn and the p channel mold MISFETQp are completed.
[0032] Next, the titanium film is deposited all over the semi-conductor substrate 1 using the sputtering method. Then, by carrying out annealing (the 1st annealing) of the semi-conductor substrate 1 at the temperature of about 650-700 degrees C among nitrogen-gas-atmosphere mind, the interface of the interface of the gate electrodes 15n and 15p and the titanium film and the source, and the drain field (the n+ semiconductor region 19, p+ semiconductor region 20) and said titanium film is made to produce a silicide-ized reaction, and the titanium silicide film 21 is formed.
[0033] Next, the silicon oxide film is deposited with a CVD method on the semi-conductor substrate 1, and an insulator layer 22 is formed by carrying out flattening of the front face using the CMP method. Furthermore, a photolithography technique is used for an insulator layer 22, and the connection hole 23 is punctured.
[0034] Then, sputter etching of the front face of the insulator layer 22 including the interior of the connection hole 23 is carried out, and the natural oxidation film formed in the front face of the front face of the insulator layer 22 including the interior of the connection hole 23 is

removed. The electric resistance between the plug 26 formed in the interior of the connection hole 23 in a next process of this sputter etching and the titanium silicide film 21 of the pars basilaris ossis occipitalis of the connection hole 23 is reduced.
[0035] next, barrier whose thickness is about 50nm on the front face of the insulator layer 22 including the interior of the connection hole 23 as shown in drawing 2 , such as titanium nitride, -- a conductor -- the film (the 1st conductivity film) 24 is deposited. this barrier -- a conductor -- if the sputtering system of the common parallel monotonous mold to deposition of the film 24 is used, since the distance between a target and a semi-conductor substrate is small, the potential difference will arise in the part into which the plasma electron generated at the time of sputtering flows into the titanium silicide film 21 through the connection hole 23, and the electron of the semi-conductor substrate 1 flows, and other parts. Consequently, the current (charge-up damage current) resulting from the potential difference may flow the semi-conductor substrate 1, and destruction or degradation of gate oxide 9 may occur. then, the collimation sputtering system shown in drawing 3 in the gestalt 1 of this operation or the long slow sputtering system shown in drawing 4 -- using -- the barrier -- a conductor -- the film 24 is deposited. Since the distance between a target and the semi-conductor substrate 1 can become large compared with the common sputtering system of an parallel monotonous mold and a collimation sputtering system and a long slow sputtering system can decrease the inflow of a up to [the semi-conductor substrate of the electron in the plasma in equipment] , they can prevent charge the titanium silicide film 21 with a plasma electron through the connection hole 23 , and can prevent the destruction or degradation of gate oxide 9 by the charge-up damage current .
[0036] moreover, a plasma electron flows into the titanium silicide film 21 through the connection hole 23, and destruction of the gate oxide 9 by the charge-up damage may take place -- the barrier -- a conductor -- it is the moment the film 24 begins to accumulate. the barrier -- a conductor -- after the film 24 accumulates to some extent, a plasma electron moves in the inside of the film of the front face of the semi-conductor substrate 1 deposited so that the potential difference within the field of the semi-conductor substrate 1 might be negated, and is not charged in the gate electrodes 15n and 15p. Therefore, since destruction of the gate oxide 9 by the charge-up damage can be prevented, the sputtering method used for deposition of the conductive film 25, 28, and 29 formed at a next process is not limited to collimation sputtering or long slow sputtering.
[0037] It could judge quantitatively that the incidence rate (percent defective) of gate oxide destruction becomes low, so that the distance between a target and a semi-conductor substrate became large as shown in drawing 5 when this invention persons investigated the relation between the distance between the target at the time of sputtering, and a semi-conductor substrate, and the incidence rate (percent defective) of gate oxide destruction by experiment. For example, although it will flow on a semi-conductor substrate so that there may be an electron in the plasma along the magnetic field of a magnet when the distance between a target and a semi-conductor substrate is 52mm as shown in drawing 6 When the distance between a target and a semi-conductor substrate is 62mm, and the distance between a target and a semi-conductor substrate was extended, in the location in which the semi-conductor substrate is installed, the effect of the magnetic field of a magnet can become small, and can decrease the inflow of a up to [the semi-conductor substrate of the electron in the plasma]. Setting in the gestalt 1 of this operation, the plasma in the chamber of a collimation sputtering system or a long slow sputtering system and the distance L between semi-conductor substrates are about 10cm. Therefore, it becomes possible to reduce further the inflow to the semi-conductor substrate 1 of the electron leading to a charge-up damage rather than the time of L being 62mm, and destruction of the gate oxide 9 by the charge-up rise damage can be further controlled or prevented rather than the time of L being 62mm.
[0038] In addition, collimation sputtering is the technique of putting in the disk by which the hole opened between a target and a semi-conductor substrate originally, cutting the slanting component of the particle by which the spatter was carried out, and raising directivity. Moreover, long slow sputtering is the technique of raising directivity by extending the distance between a

target and a semi-conductor substrate, as the component of the perpendicular direction of the particle by which the spatter was carried out is originally deposited on a semi-conductor substrate.
[0039] next, it is shown in drawing 7 -- as -- said barrier -- a conductor -- the interior of said connection hole 23 is embedded on the front face of the film 24, for example, the conductive film (the 2nd conductivity film) 25, such as a tungsten, is deposited on it. Deposition of this conductive film 25 is performed for example, with W-CVD method (equipment:, for example, AMATCentura-W).
[0040] next, it is shown in drawing 8 -- as -- the barrier on insulator layers 22 other than connection hole 23 -- a conductor -- the film 24 and the conductive film 25 are removed for example, by the CMP method, and a plug 26 is formed.
[0041] Next, as shown in drawing 9 , all over the semi-conductor substrate 1, a collimation sputtering system or a long slow sputtering system is used, for example, the conductive film (the 1st conductivity film) 27, such as titanium nitride, is deposited. Since the conductive film 27 is deposited with a collimation sputtering system or a long slow sputtering system and it becomes possible [reducing the inflow to the semi-conductor substrate 1 of the electron which can prevent a plasma electron flowing into a plug 26, and causes a charge-up damage], it can prevent the gate oxide 9 by the charge-up rise damage breaking.
[0042] Then, the conductive film (the 2nd conductivity film) 28, such as aluminum, is deposited on the front face of the conductive film 27. Furthermore, the conductive film 29, such as titanium nitride, is continuously deposited on the front face of the conductive film 28. In case this conductive film 29 carries out patterning of the conductive film 27, the conductive film 28, and the conductive film 29 according to a photolithography process, it has the function which prevents the scattered reflection of light. Deposition of the conductive film 28 and the conductive film 29 is a collimation sputtering system and parallel monotonous mold magnetron sputtering systems Endura other than a long slow sputtering system, for example, AMAT. It carries out by the sputtering method using HP.
[0043] Next, as shown in drawing 10 , the conductive film 27, the conductive film 28, and the conductive film 29 are processed using a dry etching technique, and wiring 30 is formed.
[0044] Next, as shown in drawing 11 , according to the process explained using drawing 1 - drawing 10 , and the same process, an insulator layer 31, the connection hole 32, a plug 33, and wiring 34 are formed, and the semiconductor integrated circuit equipment of the gestalt 1 of this operation is manufactured. In addition, wiring may be further formed in the upper part of wiring 34 at a multilayer.
[0045] According to the manufacture approach of the semiconductor integrated circuit equipment of the gestalt 1 this operation, since destruction of said gate oxide 9 by the charge-up rise damage can be prevented, the yield and dependability of semiconductor integrated circuit equipment can be improved.
[0046] (Gestalt 2 of operation) the barrier [in / in the manufacture approach of the semiconductor integrated circuit equipment of the gestalt 2 this operation / the gestalt 1 of said operation] -- a conductor -- on the occasion of deposition processing of the film 24 and the conductive film 27, the sputtering method of another low damage conditions is used. Since other processes and members are the same as that of the gestalt 1 of said operation, the explanation about the same process as them and a member is omitted.
[0047] The manufacture approach of the semiconductor integrated circuit equipment of the gestalt 2 this operation is explained using drawing 12 - drawing 14 .
[0048] The process of the manufacture approach of the semiconductor integrated circuit equipment of the gestalt 2 this operation explained using drawing 1 in the gestalt 1 of said operation is the same.
[0049] then, the front face of the insulator layer 22 which includes the interior of the connection hole 23 as shown in drawing 12 which expanded the connection hole 23 neighborhood -- for example, barrier, such as titanium nitride, -- a conductor -- film 24a is deposited. this barrier -- a conductor -- film 24a is deposited with the sputtering system which has the chamber from which the distance (T/S) between a target and the semi-conductor substrate 1 is set to about

5cm (1st sputtering process). this invention persons investigated the pressure of the argon gas at the time of sputtering which does not destroy gate oxide 9 at the time of T/S=5cm by experiment. Consequently, as shown in drawing 13 , when carrying out the pressure of argon gas to more than about 7 mTorr(s) (**0.931Pa), since even the semi-conductor substrate 1 stops being able to arrive easily and the plasma electron stopped being able to flow into the titanium silicide film 21 easily in order to repeat an argon atom and a collision and to melt, by the time it reaches the semi-conductor substrate 1, it became clear that destruction of the gate oxide 9 by the charge-up damage does not occur. At this time, the electron in the plasma in a chamber is expressed with c (time), then c=L/lambda in the count which will collide with an argon by the time it reaches a semi-conductor substrate. Here, it is L=T/S (cm), and lambda is an electronic mean free path and is expressed with lambda=10-2/P (cm). P is the pressure (a unit is Torr) of argon gas. P from which c becomes 3.5 times on count, and c becomes 4 times or more in fact since gate oxide is not destroyed [according to investigation of this invention person] in the conditions from which P becomes more than about 7 mTorr(s) (**0.931Pa) in the case of T/S=5cm -- the barrier -- a conductor -- what is necessary is just to deposit film 24a the gestalt 2 of this operation -- setting -- the barrier -- a conductor -- P at the time of depositing film 24a is taken as about 8 mTorr(s) (**1.064Pa). moreover, the gestalt 1 of said operation -- setting -- the barrier -- a conductor -- it is the moment it begins to form membranes on the front face of the insulator layer 22 including the interior of the connection hole 23 that destruction of the gate oxide 9 by the charge-up damage may take place by the sputtering method for the reason which the process which deposits the film 24 explained by the way, and the same reason. the gestalt 2 of this operation -- setting -- the barrier -- a conductor -- the thickness of film 24a -- for example, the barrier -- a conductor -- the thickness of film 24a, and the barrier mentioned later -- a conductor -- since it carries out to about about 1 of total value with the thickness of film 24b / 10 and the total value is about 50nm -- the barrier -- a conductor -- the thickness of film 24a may be about 5nm preferably. In addition, that what is necessary is just to set up P so that c may become 4 times or more in other than T/S=5cm, since it is c=L/lambda, L=T/S, and lambda=10-2/P, it can be referred to as P=cx10-2/L, 4 can be substituted for c, the concrete numeric value of L can be substituted, and the minimum value of P can be calculated.

[0050] next, it is shown in drawing 14 -- as -- said barrier -- a conductor -- the front face of film 24a -- for example, barrier, such as titanium nitride, -- a conductor -- film 24b -- about 45nm -- depositing -- said barrier -- a conductor -- film 24a and said barrier -- a conductor -- the barrier whose thickness film 24b is doubled and is about 50nm -- a conductor -- it considers as the film 24. the barrier -- a conductor -- deposition of film 24b -- the sputtering method -- using -- said barrier -- a conductor -- a pressure lower than the argon gas pressure when depositing film 24a -- depositing (2nd sputtering process) -- said barrier -- a conductor -- you may deposit by the argon gas pressure when depositing film 24a, and the pressure below comparable.

[0051] Then, after forming a plug 26 at the process explained using drawing 7 and drawing 8 in the gestalt 1 of said operation, and the same process and depositing an insulator layer 31, the conductive film 27, such as titanium nitride, is deposited by the sputtering method all over the semi-conductor substrate 1. this time -- the gestalt 2 of this about 5nm operation of the beginning of said conductive film 27 -- setting -- said barrier -- a conductor -- it deposits on the same conditions as the conditions when depositing film 24a, and can prevent said gate oxide 9 by the charge-up rise damage breaking. moreover, said all conductive film 27 -- said barrier -- a conductor -- you may deposit on the same conditions as the conditions when depositing film 24a.

[0052] Then, wiring 30 is formed by depositing and carrying out patterning of the conductive film 28 and the conductive film 29 at the process explained using drawing 9 and drawing 10 in the gestalt 1 of said operation, and the same process.

[0053] Then, after forming an insulator layer 31 and the connection hole 32 at the process explained using drawing 11 in the gestalt 1 of said operation, and the same process, according to said plug 26 explained in the gestalt 2 of this operation, and the formation process of said wiring

30 and the same process, a plug 33 and wiring 34 are formed and the semiconductor integrated circuit equipment of the gestalt 2 of this operation is manufactured.
[0054] (Gestalt 3 of operation) the barrier [in / in the manufacture approach of the semiconductor integrated circuit equipment of the gestalt 3 this operation / the gestalten 1 or 2 of said operation] -- a conductor -- the sputtering method of still more nearly another low damage conditions is used for deposition of the film 24 and the conductive film 27. Other processes and members are the same as that of the gestalten 1 or 2 of operation, and the explanation about the same process as them and a member is omitted.
[0055] The manufacture approach of the semiconductor integrated circuit equipment of the gestalt 3 this operation is explained according to drawing 15 . The process of the manufacture approach of the semiconductor integrated circuit equipment of the gestalt 3 this operation explained using drawing 1 in the gestalt 1 of said operation is the same.
[0056] then, the front face of the insulator layer 22 including the interior of the connection hole 23 -- for example, barrier, such as titanium nitride, -- a conductor -- film 24a -- parallel monotonous mold magnetron sputtering system Endura, for example, AMAT, It deposits by the sputtering method using HP. It turned out that relation (it is a source from the 1996 spring Japan Society of Applied Physics (Toshiba data)) between the amounts Qbd (C/cm2) of charges in case the temperature and gate oxide of the semi-conductor substrate 1 break as shown in drawing 15 is, and the amount of charges in case gate oxide 9 breaks with the rise of the temperature of the semi-conductor substrate 1 also becomes small. that is, -- since it becomes easy to destroy gate oxide 9 with the rise of the temperature of the semi-conductor substrate 1 -- the barrier -- a conductor -- in case film 24a is deposited, temperature of the semi-conductor substrate 1 is made into about 100 degrees C or less (1st sputtering process). In addition, Tox in drawing 15 is the thickness of gate oxide 9. moreover -- since it may happen in the gestalt 3 of this operation that destruction of the gate oxide 9 by the charge-up damage may take place at the moment of beginning to form membranes by the sputtering method on the front face of the insulator layer 22 including the interior of the connection hole 23 -- the barrier -- a conductor -- the thickness of film 24a may be about 5nm.
[0057] next, the barrier -- a conductor -- the front face of film 24a -- for example, barrier, such as titanium nitride, -- a conductor -- film 24b -- about 45nm -- depositing -- the barrier -- a conductor -- film 24a and the barrier -- a conductor -- the barrier whose thickness film 24b is doubled and is about 50nm -- a conductor -- it considers as the film 24. the barrier -- a conductor -- deposition of film 24b -- parallel monotonous mold magnetron sputtering system Endura, for example, AMAT, the sputtering method using HP -- using -- the temperature of the semi-conductor substrate 1 in that case -- the barrier -- a conductor -- it may be higher than the temperature of the semi-conductor substrate 1 when depositing film 24a (2nd sputtering process).
[0058] Then, after forming a plug 26 at the process explained using drawing 7 and drawing 8 in the gestalt 1 of said operation, and the same process, the conductive film 27, such as titanium nitride, is deposited by the sputtering method all over the semi-conductor substrate 1. this time -- the gestalt 3 of this about 5nm operation of the beginning of the conductive film 27 -- setting -- the barrier -- a conductor -- it can prevent the gate oxide 9 by the charge-up rise damage breaking by depositing on the same conditions as the conditions when depositing film 24a. moreover, all the conductive film 27 -- the barrier -- a conductor -- you may deposit on the same conditions as the conditions when depositing film 24a.
[0059] Then, wiring 30 is formed by depositing and carrying out patterning of the conductive film 28 and the conductive film 29 at the process explained using drawing 9 and drawing 10 in the gestalt 1 of said operation, and the same process.
[0060] Then, after forming an insulator layer 31 and the connection hole 32 at the process explained using drawing 11 in the gestalt 1 of said operation, and the same process, according to the plug 26 explained in the gestalt 3 of this operation, and the formation process of wiring 30 and the same process, a plug 33 and wiring 34 are formed and the semiconductor integrated circuit equipment of the gestalt 3 of this operation is manufactured.
[0061] As mentioned above, although invention made by this invention person was concretely

explained based on the gestalt of implementation of invention, it cannot be overemphasized that it can change variously in the range which this invention is not limited to the gestalt of said operation, and does not deviate from the summary.

[0062] For example, in the gestalt 1 of operation, although Salicide was performed using the titanium film and the titanium silicide film was formed, a silicide-ized reaction may be produced using the tungsten film, the molybdenum film, the tantalum film, or the cobalt film.

[0063]

[Effect of the Invention] It will be as follows if the effectiveness acquired by the typical thing among invention indicated by this application is explained briefly.

(1) According to this invention, the inflow to the semi-conductor substrate of the plasma electron generated in case a thin film is deposited by the sputtering method can be reduced, and destruction of the gate oxide by the charge-up damage can be prevented.

(2) Since destruction of the gate oxide by the charge up of the plasma electron at the time of depositing a thin film by the sputtering method can be prevented according to this invention, the yield and dependability of semiconductor integrated circuit equipment can be improved.

[Translation done.]

* NOTICES *

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TECHNICAL FIELD

[Field of the Invention] About the manufacturing technology of semiconductor integrated circuit equipment, by the sputtering method which used the plasma, especially this invention is applied to the manufacturing technology of the semiconductor integrated circuit equipment which a thin film deposits, and relates to an effective technique.

[Translation done.]

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PRIOR ART

[Description of the Prior Art] In the thin film formation process of semiconductor integrated circuit equipment of having MISFET (Metal Insulator Semiconductor Field Effect Transistor), as for most about the membrane formation performed by the sputtering method, the magnetron sputtering method has been used for improvement in the speed of thin film formation, for example as indicated by November 22, 1991, "1992 Edition VLSI manufacture and a testing-device guidebook" of Kogyo Chosakai Publishing Issue, and p84-p93.
[0003] Since the current magnetron sputtering method has the thing of the system which the plasma can generate and form with mainly comparatively low gas pressure in use and the (a) low battery and the ideal discharge property of a high current are acquired Since the atom by which (b) spatter whose sputtering effectiveness per power consumption improves is carried out reaches efficiently the semi-conductor substrate countered and arranged Since the collision of the electron to (c) semi-conductor substrate in which membrane formation at a high speed is possible can be reduced, the rise of the temperature of a semi-conductor substrate is reduced and it has the description of ** in which membrane formation at low temperature is possible.

[Translation done.]

EFFECT OF THE INVENTION

[Effect of the Invention] It will be as follows if the effectiveness acquired by the typical thing among invention indicated by this application is explained briefly.
(1) According to this invention, the inflow to the semi-conductor substrate of the plasma electron generated in case a thin film is deposited by the sputtering method can be reduced, and destruction of the gate oxide by the charge-up damage can be prevented.
(2) Since destruction of the gate oxide by the charge up of the plasma electron at the time of depositing a thin film by the sputtering method can be prevented according to this invention, the yield and dependability of semiconductor integrated circuit equipment can be improved.

[Translation done.]

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] However, this invention persons found out producing the following problems in the Prior art which deposits a thin film by the magnetron sputtering method for using plasma equipment.
[0005] That is, the electron in the plasma flows on a semi-conductor substrate so that the magnetic field of a magnet may be met. This electron that flowed is accumulated in a semi-conductor substrate, and the potential difference arises in the part into which the electron of a semi-conductor substrate flows, and other parts. When the current (damage current) resulting from this potential difference flows a semi-conductor substrate, the gate oxide of MISFET formed on the principal plane of a semi-conductor substrate may break or deteriorate. Therefore, it is necessary to cope with the sputtering system which uses the plasma and to use the spatter chamber and process which check the inflow to an electronic semi-conductor substrate.
[0006] The purpose of this invention is to offer the technique which deposits a thin film by the sputtering method using the plasma, without destroying or deteriorating the gate oxide of MISFET.
[0007] The other purposes and the new description will become clear from description and the accompanying drawing of this specification along [said] this invention.

[Translation done.]

MEANS

[Means for Solving the Problem] It will be as follows if the outline of a typical thing is briefly explained among invention indicated in this application.
[0009] That is, in case this invention deposits the conductive film on the front face of the insulator layer deposited on the principal plane of a semi-conductor substrate after puncturing a connection hole, the 1st and 2nd sputtering processes are included in order, and said 1st sputtering process is the sputtering method which controls the inflow to said semi-conductor substrate of the electron generated in sputtering.
[0010] Moreover, said 1st conductivity film deposits including the process which deposits the 1st conductivity film by the sputtering method, and the process which deposits the 2nd conductivity film used as the main conductive layer on the front face of said 1st conductivity film on the sputtering conditions which control the inflow to said semi-conductor substrate of the electron generated in sputtering after this invention's puncturing a connection hole on the front face of the insulator layer deposited on the principal plane of a semi-conductor substrate.
[0011] Moreover, said 1st conductivity film is deposited by the collimation sputtering method including the process which deposits the 1st conductivity film by the sputtering method, and the process which deposits the 2nd conductivity film used as the main conductive layer on the front face of said 1st conductivity film after this invention's puncturing a connection hole on the front face of the insulator layer deposited on the principal plane of a semi-conductor substrate.
[0012] Moreover, said 1st conductivity film is deposited by the long slow sputtering method including the process which deposits the 1st conductivity film by the sputtering method, and the process which deposits the 2nd conductivity film used as the main conductive layer on the front face of said 1st conductivity film after this invention's puncturing a connection hole on the front face of the insulator layer deposited on the principal plane of a semi-conductor substrate.
[0013] Moreover, the process which deposits the 1st conductivity film by the sputtering method after this invention's puncturing a connection hole on the front face of the insulator layer deposited on the principal plane of a semi-conductor substrate, It is a thing including the process which deposits the 2nd conductivity film used as the main conductive layer on the front face of said 1st conductivity film. Said 1st conductivity film In order to prevent the electron generated in sputtering flowing into said semi-conductor substrate, it deposits by the sputtering method of the discharge-gas-pressure force of colliding with argon gas at least 4 times or more by the time a plasma electron reaches a semi-conductor substrate.
[0014] Moreover, said 1st conductivity film is deposited including the process which deposits the 1st conductivity film by the sputtering method, and the process which deposits the 2nd conductivity film used as the main conductive layer on the front face of said 1st conductivity film by the sputtering method under the conditions which made temperature of said semi-conductor substrate 100 degrees C or less after this invention's puncturing a connection hole on the front face of the insulator layer deposited on the principal plane of a semi-conductor substrate.
[0015] Moreover, in case this invention deposits the conductive film on the front face of said insulator layer containing said plug after forming a plug in the insulator layer deposited on the principal plane of a semi-conductor substrate, it includes the 1st and 2nd sputtering processes

in order, and said 1st sputtering process is the sputtering method which controls the inflow to said semi-conductor substrate of the electron generated in sputtering.
[0016] Moreover, the process which deposits the 1st conductivity film on the front face of said insulator layer containing said plug by the sputtering method after this invention forms a plug in the insulator layer deposited on the principal plane of a semi-conductor substrate, Said 1st conductivity film is deposited including the process which deposits the 2nd conductivity film used as the main conductive layer on the front face of said 1st conductivity film on the sputtering conditions which control the inflow to said semi-conductor substrate of the electron generated in sputtering.
[0017] Since it can prevent the plasma electron generated at the time of sputtering flowing into a gate electrode through a connection hole in case the conductive film is deposited at the 1st sputtering process on the insulator layer containing a connection hole according to above-mentioned this invention, it can prevent the potential difference arising in the part into which the electron of a semi-conductor substrate flows, and other parts. Consequently, since the current (charge-up damage current) resulting from said potential difference can prevent flowing said semi-conductor substrate, the destruction or degradation of the gate oxide of MISFET formed on the principal plane of said semi-conductor substrate can be prevented, and the yield and dependability of semiconductor integrated circuit equipment can be raised.
[0018] Moreover, even said semi-conductor substrate can make it hard to reach a plasma electron on the insulator layer containing a connection hole by making the 1st conductivity film into the discharge-gas-pressure force of colliding the sputtering method with an argon atom at least 4 times or more by the time a plasma electron reaches a semi-conductor substrate in case it uses and deposits according to above-mentioned this invention. Consequently, since it can prevent a plasma electron flowing into a gate electrode through a connection hole, the destruction or degradation of the gate oxide of MISFET resulting from a charge-up damage current flowing can be prevented, and the yield and dependability of semiconductor integrated circuit equipment can be raised.
[0019] Moreover, according to above-mentioned this invention, the amount value of charges since the sputtering method is used and deposited, in case the gate oxide of MISFET destroys the 1st conductivity film on the insulator layer which contains a connection hole under the conditions which made temperature of a semi-conductor substrate 100 degrees C or less can be improved. Consequently, the destruction or degradation of said gate oxide resulting from a charge-up damage current can be prevented, and the yield and dependability of semiconductor integrated circuit equipment can be raised.
[0020]
[Embodiment of the Invention] Hereafter, the gestalt of operation of this invention is explained to a detail based on a drawing. In addition, in the complete diagram for explaining the gestalt of operation, the same sign is given to the member which has the same function, and explanation of the repeat is omitted.
[0021] (Gestalt 1 of operation) The gestalt 1 of this operation applies this invention to the manufacture approach of the semiconductor integrated circuit equipment constituted from an n channel mold MISFETQn and a p channel mold MISFETQp.
[0022] Hereafter, the manufacture approach of the above-mentioned semiconductor integrated circuit equipment is explained in order of a process using drawing 1 - drawing 9 .
[0023] First, as shown in drawing 1 , the semi-conductor substrate 1 which consists of single crystal silicon whose specific resistance is about 10ohmcm is heat-treated at about 850 degrees C. The thin silicon oxide film (pad oxide film) of about 10nm of thickness is formed in the principal plane. subsequently, this silicon oxide film top -- the silicon nitride film of about 120nm of thickness -- CVD (Chemical Vapor Deposition), after depositing in law The silicon nitride film and silicon oxide film of a component isolation region are removed by the dry etching which used the photoresist film as the mask. When densifying the silicon oxide film embedded to the interior of an isolation slot at a next process (biscuit ware), the silicon oxide film is formed in order to ease the stress which joins a substrate. Moreover, since a silicon nitride film has the property which cannot oxidize easily, it is used as a mask which prevents oxidation on the front face of a

substrate of the lower part (active region).
[0024] Then, after forming a slot with a depth of about 350nm in the semi-conductor substrate 1 of a component isolation region by the dry etching which used the silicon nitride film as the mask, in order to remove the damage layer produced in the wall of a slot by etching, the semi-conductor substrate 1 is heat-treated at about 1000 degrees C, and the thin silicon oxide film 5 of about 10nm of thickness is formed in the wall of a slot.
[0025] Then, in order to deposit the silicon oxide film 6 of about 380nm of thickness with a CVD method on the semi-conductor substrate 1 and to improve the membraneous quality of the silicon oxide film 6 subsequently, the semi-conductor substrate 1 is heat-treated and the silicon oxide film 6 is densified (eye thermal shrinking). then, chemical mechanical polishing (Chemical Mechanical Polishing;CMP) which used the silicon nitride film for the stopper -- a front face forms the isolation slot 4 by which flattening was carried out by grinding the silicon oxide film 6 by law, and leaving the interior of a slot.
[0026] then, the field which forms the n channel mold MISFET of the semi-conductor substrate 1 after removing the silicon nitride film which remained on the active region of the semi-conductor substrate 1 by the wet etching using a heat phosphoric acid -- B (boron) -- an ion implantation -- carrying out -- p mold -- the field which forms a well 7 and forms the p channel mold MISFET -- P (Lynn) -- an ion implantation -- carrying out -- n mold -- a well 8 is formed.
[0027] then, p mold -- a well 7 and n mold -- the semi-conductor substrate 1 after removing the silicon oxide film of each front face of a well 8 using the penetrant remover of HF (fluoric acid) system -- wet oxidation -- carrying out -- p mold -- a well 7 and n mold -- pure gate oxide 9 of about 3.5nm of thickness is formed in each front face of a well 8.
[0028] Next, the non dope polycrystalline silicon film of about 90-100nm of thickness is deposited with a CVD method on the semi-conductor substrate 1. Then, using the mask of an ion notes necessity, the ion implantation of the P (Lynn) is carried out to the non dope polycrystalline silicon film of the upper part of a well 7 p molds, and n mold polycrystalline silicon film is formed. Furthermore it continues, the ion implantation of the B (boron) is carried out to the non dope polycrystalline silicon film of a well 8 n molds using the mask of an ion notes necessity, and p mold polycrystalline silicon film is formed.
[0029] Next, the photoresist film is used as a mask and dry etching of n mold polycrystalline silicon film and the p mold polycrystalline silicon film is carried out. 15n of gate electrodes of the n channel mold MISFET which consists of n mold polycrystalline silicon is formed in the upper part of the gate oxide 9 of a well 7 p molds by this, and gate electrode 15p of the p channel mold MISFET which consists of p mold polycrystalline silicon film is formed in the upper part of the gate oxide 9 of a well 8 n molds. The gate length of 15n of gate electrodes and gate electrode 15p is 0.25 micrometers.
[0030] Next, after removing the photoresist film used for processing of the gate electrodes 15n and 15p, n-mold semiconductor region 16 is formed in a well 7. p mold -- a well 7 -- n mold impurity (Lynn), for example, P, -- an ion implantation -- carrying out -- p mold of the both sides of 15n of gate electrodes -- n mold -- a well 8 -- p mold impurity (boron), for example, B, -- an ion implantation -- carrying out -- n mold of the both sides of gate electrode 15p -- p-mold semiconductor region 17 is formed in a well 8.
[0031] next, the semi-conductor substrate 1 top -- the silicon oxide film of about 100nm of thickness -- a CVD method -- depositing -- reactive ion etching (RIE) -- the sidewall spacer 18 is formed in 15n of gate electrodes of the n channel mold MISFET, and each side attachment wall of gate electrode 15p of the p channel mold MISFET by carrying out anisotropic etching of this silicon oxide film using law. then, p mold -- a well 7 -- n mold impurity (arsenic), for example, As, -- an ion implantation -- carrying out -- n+ mold semiconductor region 19 (the source, drain) of the n channel mold MISFET -- forming -- n mold -- the ion implantation of p mold impurity (boron), for example, the B, is carried out to a well 8, and p+ mold semiconductor region 20 (the source, drain) of the p channel mold MISFET is formed. Thereby, the source of LDD (Lightly Doped Drain) structure and a drain field are formed in each of the n channel mold MISFET and the p channel mold MISFET, and the n channel mold MISFETQn and the p channel mold MISFETQp are completed.

[0032] Next, the titanium film is deposited all over the semi-conductor substrate 1 using the sputtering method. Then, by carrying out annealing (the 1st annealing) of the semi-conductor substrate 1 at the temperature of about 650-700 degrees C among nitrogen-gas-atmosphere mind, the interface of the interface of the gate electrodes 15n and 15p and the titanium film and the source, and the drain field (the n+ semiconductor region 19, p+ semiconductor region 20) and said titanium film is made to produce a silicide-ized reaction, and the titanium silicide film 21 is formed.
[0033] Next, the silicon oxide film is deposited with a CVD method on the semi-conductor substrate 1, and an insulator layer 22 is formed by carrying out flattening of the front face using the CMP method. Furthermore, a photolithography technique is used for an insulator layer 22, and the connection hole 23 is punctured.
[0034] Then, sputter etching of the front face of the insulator layer 22 including the interior of the connection hole 23 is carried out, and the natural oxidation film formed in the front face of the front face of the insulator layer 22 including the interior of the connection hole 23 is removed. The electric resistance between the plug 26 formed in the interior of the connection hole 23 in a next process of this sputter etching and the titanium silicide film 21 of the pars basilaris ossis occipitalis of the connection hole 23 is reduced.
[0035] next, barrier whose thickness is about 50nm on the front face of the insulator layer 22 including the interior of the connection hole 23 as shown in drawing 2 , such as titanium nitride, -- a conductor -- the film (the 1st conductivity film) 24 is deposited. this barrier -- a conductor -- if the sputtering system of the common parallel monotonous mold to deposition of the film 24 is used, since the distance between a target and a semi-conductor substrate is small, the potential difference will arise in the part into which the plasma electron generated at the time of sputtering flows into the titanium silicide film 21 through the connection hole 23, and the electron of the semi-conductor substrate 1 flows, and other parts. Consequently, the current (charge-up damage current) resulting from the potential difference may flow the semi-conductor substrate 1, and destruction or degradation of gate oxide 9 may occur. then, the collimation sputtering system shown in drawing 3 in the gestalt 1 of this operation or the long slow sputtering system shown in drawing 4 -- using -- the barrier -- a conductor -- the film 24 is deposited. Since the distance between a target and the semi-conductor substrate 1 can become large compared with the common sputtering system of an parallel monotonous mold and a collimation sputtering system and a long slow sputtering system can decrease the inflow of a up to [the semi-conductor substrate of the electron in the plasma in equipment] , they can prevent charge the titanium silicide film 21 with a plasma electron through the connection hole 23 , and can prevent the destruction or degradation of gate oxide 9 by the charge-up damage current .
[0036] moreover, a plasma electron flows into the titanium silicide film 21 through the connection hole 23, and destruction of the gate oxide 9 by the charge-up damage may take place -- the barrier -- a conductor -- it is the moment the film 24 begins to accumulate. the barrier -- a conductor -- after the film 24 accumulates to some extent, a plasma electron moves in the inside of the film of the front face of the semi-conductor substrate 1 deposited so that the potential difference within the field of the semi-conductor substrate 1 might be negated, and is not charged in the gate electrodes 15n and 15p. Therefore, since destruction of the gate oxide 9 by the charge-up damage can be prevented, the sputtering method used for deposition of the conductive film 25, 28, and 29 formed at a next process is not limited to collimation sputtering or long slow sputtering.
[0037] It could judge quantitatively that the incidence rate (percent defective) of gate oxide destruction becomes low, so that the distance between a target and a semi-conductor substrate became large as shown in drawing 5 when this invention persons investigated the relation between the distance between the target at the time of sputtering, and a semi-conductor substrate, and the incidence rate (percent defective) of gate oxide destruction by experiment. For example, although it will flow on a semi-conductor substrate so that there may be an electron in the plasma along the magnetic field of a magnet when the distance between a target and a semi-conductor substrate is 52mm as shown in drawing 6 When the distance between a

target and a semi-conductor substrate is 62mm, and the distance between a target and a semi-conductor substrate was extended, in the location in which the semi-conductor substrate is installed, the effect of the magnetic field of a magnet can become small, and can decrease the inflow of a up to [the semi-conductor substrate of the electron in the plasma]. Setting in the gestalt 1 of this operation, the plasma in the chamber of a collimation sputtering system or a long slow sputtering system and the distance L between semi-conductor substrates are about 10cm. Therefore, it becomes possible to reduce further the inflow to the semi-conductor substrate 1 of the electron leading to a charge-up damage rather than the time of L being 62mm, and destruction of the gate oxide 9 by the charge-up rise damage can be further controlled or prevented rather than the time of L being 62mm.

[0038] In addition, collimation sputtering is the technique of putting in the disk by which the hole opened between a target and a semi-conductor substrate originally, cutting the slanting component of the particle by which the spatter was carried out, and raising directivity. Moreover, long slow sputtering is the technique of raising directivity by extending the distance between a target and a semi-conductor substrate, as the component of the perpendicular direction of the particle by which the spatter was carried out is originally deposited on a semi-conductor substrate.

[0039] next, it is shown in drawing 7 -- as -- said barrier -- a conductor -- the interior of said connection hole 23 is embedded on the front face of the film 24, for example, the conductive film (the 2nd conductivity film) 25, such as a tungsten, is deposited on it. Deposition of this conductive film 25 is performed for example, with W-CVD method (equipment:, for example, AMATCentura-W).

[0040] next, it is shown in drawing 8 -- as -- the barrier on insulator layers 22 other than connection hole 23 -- a conductor -- the film 24 and the conductive film 25 are removed for example, by the CMP method, and a plug 26 is formed.

[0041] Next, as shown in drawing 9 , all over the semi-conductor substrate 1, a collimation sputtering system or a long slow sputtering system is used, for example, the conductive film (the 1st conductivity film) 27, such as titanium nitride, is deposited. Since the conductive film 27 is deposited with a collimation sputtering system or a long slow sputtering system and it becomes possible [reducing the inflow to the semi-conductor substrate 1 of the electron which can prevent a plasma electron flowing into a plug 26, and causes a charge-up damage], it can prevent the gate oxide 9 by the charge-up rise damage breaking.

[0042] Then, the conductive film (the 2nd conductivity film) 28, such as aluminum, is deposited on the front face of the conductive film 27. Furthermore, the conductive film 29, such as titanium nitride, is continuously deposited on the front face of the conductive film 28. In case this conductive film 29 carries out patterning of the conductive film 27, the conductive film 28, and the conductive film 29 according to a photolithography process, it has the function which prevents the scattered reflection of light. Deposition of the conductive film 28 and the conductive film 29 is a collimation sputtering system and parallel monotonous mold magnetron sputtering systems Endura other than a long slow sputtering system, for example, AMAT. It carries out by the sputtering method using HP.

[0043] Next, as shown in drawing 10 , the conductive film 27, the conductive film 28, and the conductive film 29 are processed using a dry etching technique, and wiring 30 is formed.

[0044] Next, as shown in drawing 11 , according to the process explained using drawing 1 - drawing 10 , and the same process, an insulator layer 31, the connection hole 32, a plug 33, and wiring 34 are formed, and the semiconductor integrated circuit equipment of the gestalt 1 of this operation is manufactured. In addition, wiring may be further formed in the upper part of wiring 34 at a multilayer.

[0045] According to the manufacture approach of the semiconductor integrated circuit equipment of the gestalt 1 this operation, since destruction of said gate oxide 9 by the charge-up rise damage can be prevented, the yield and dependability of semiconductor integrated circuit equipment can be improved.

[0046] (Gestalt 2 of operation) the barrier [in / in the manufacture approach of the semiconductor integrated circuit equipment of the gestalt 2 this operation / the gestalt 1 of said

operation] -- a conductor -- on the occasion of deposition processing of the film 24 and the conductive film 27, the sputtering method of another low damage conditions is used. Since other processes and members are the same as that of the gestalt 1 of said operation, the explanation about the same process as them and a member is omitted.
[0047] The manufacture approach of the semiconductor integrated circuit equipment of the gestalt 2 this operation is explained using drawing 12 - drawing 14 .
[0048] The process of the manufacture approach of the semiconductor integrated circuit equipment of the gestalt 2 this operation explained using drawing 1 in the gestalt 1 of said operation is the same.
[0049] then, the front face of the insulator layer 22 which includes the interior of the connection hole 23 as shown in drawing 12 which expanded the connection hole 23 neighborhood -- for example, barrier, such as titanium nitride, -- a conductor -- film 24a is deposited. this barrier -- a conductor -- film 24a is deposited with the sputtering system which has the chamber from which the distance (T/S) between a target and the semi-conductor substrate 1 is set to about 5cm (1st sputtering process). this invention persons investigated the pressure of the argon gas at the time of sputtering which does not destroy gate oxide 9 at the time of T/S=5cm by experiment. Consequently, as shown in drawing 13 , when carrying out the pressure of argon gas to more than about 7 mTorr(s) (**0.931Pa), since even the semi-conductor substrate 1 stops being able to arrive easily and the plasma electron stopped being able to flow into the titanium silicide film 21 easily in order to repeat an argon atom and a collision and to melt, by the time it reaches the semi-conductor substrate 1, it became clear that destruction of the gate oxide 9 by the charge-up damage does not occur. At this time, the electron in the plasma in a chamber is expressed with c (time), then c=L/lambda in the count which will collide with an argon by the time it reaches a semi-conductor substrate. Here, it is L=T/S (cm), and lambda is an electronic mean free path and is expressed with lambda=10-2/P (cm). P is the pressure (a unit is Torr) of argon gas. P from which c becomes 3.5 times on count, and c becomes 4 times or more in fact since gate oxide is not destroyed [according to investigation of this invention person] in the conditions from which P becomes more than about 7 mTorr(s) (**0.931Pa) in the case of T/S=5cm -- the barrier -- a conductor -- what is necessary is just to deposit film 24a the gestalt 2 of this operation -- setting -- the barrier -- a conductor -- P at the time of depositing film 24a is taken as about 8 mTorr(s) (**1.064Pa). moreover, the gestalt 1 of said operation -- setting -- the barrier -- a conductor -- it is the moment it begins to form membranes on the front face of the insulator layer 22 including the interior of the connection hole 23 that destruction of the gate oxide 9 by the charge-up damage may take place by the sputtering method for the reason which the process which deposits the film 24 explained by the way, and the same reason. the gestalt 2 of this operation -- setting -- the barrier -- a conductor -- the thickness of film 24a -- for example, the barrier -- a conductor -- the thickness of film 24a, and the barrier mentioned later -- a conductor -- since it carries out to about about 1 of total value with the thickness of film 24b / 10 and the total value is about 50nm -- the barrier -- a conductor -- the thickness of film 24a may be about 5nm preferably. In addition, that what is necessary is just to set up P so that c may become 4 times or more in other than T/S=5cm, since it is c=L/lambda, L=T/S, and lambda=10-2/P, it can be referred to as P=cx10-2/L, 4 can be substituted for c, the concrete numeric value of L can be substituted, and the minimum value of P can be calculated.
[0050] next, it is shown in drawing 14 -- as -- said barrier -- a conductor -- the front face of film 24a -- for example, barrier, such as titanium nitride, -- a conductor -- film 24b -- about 45nm -- depositing -- said barrier -- a conductor -- film 24a and said barrier -- a conductor -- the barrier whose thickness film 24b is doubled and is about 50nm -- a conductor -- it considers as the film 24. the barrier -- a conductor -- deposition of film 24b -- the sputtering method -- using -- said barrier -- a conductor -- a pressure lower than the argon gas pressure when depositing film 24a -- depositing (2nd sputtering process) -- said barrier -- a conductor -- you may deposit by the argon gas pressure when depositing film 24a, and the pressure below comparable.
[0051] Then, after forming a plug 26 at the process explained using drawing 7 and drawing 8 in

the gestalt 1 of said operation, and the same process and depositing an insulator layer 31, the conductive film 27, such as titanium nitride, is deposited by the sputtering method all over the semi-conductor substrate 1. this time -- the gestalt 2 of this about 5nm operation of the beginning of said conductive film 27 -- setting -- said barrier -- a conductor -- it deposits on the same conditions as the conditions when depositing film 24a, and can prevent said gate oxide 9 by the charge-up rise damage breaking. moreover, said all conductive film 27 -- said barrier -- a conductor -- you may deposit on the same conditions as the conditions when depositing film 24a.

[0052] Then, wiring 30 is formed by depositing and carrying out patterning of the conductive film 28 and the conductive film 29 at the process explained using drawing 9 and drawing 10 in the gestalt 1 of said operation, and the same process.

[0053] Then, after forming an insulator layer 31 and the connection hole 32 at the process explained using drawing 11 in the gestalt 1 of said operation, and the same process, according to said plug 26 explained in the gestalt 2 of this operation, and the formation process of said wiring 30 and the same process, a plug 33 and wiring 34 are formed and the semiconductor integrated circuit equipment of the gestalt 2 of this operation is manufactured.

[0054] (Gestalt 3 of operation) the barrier [in / in the manufacture approach of the semiconductor integrated circuit equipment of the gestalt 3 this operation / the gestalten 1 or 2 of said operation] -- a conductor -- the sputtering method of still more nearly another low damage conditions is used for deposition of the film 24 and the conductive film 27. Other processes and members are the same as that of the gestalten 1 or 2 of operation, and the explanation about the same process as them and a member is omitted.

[0055] The manufacture approach of the semiconductor integrated circuit equipment of the gestalt 3 this operation is explained according to drawing 15 . The process of the manufacture approach of the semiconductor integrated circuit equipment of the gestalt 3 this operation explained using drawing 1 in the gestalt 1 of said operation is the same.

[0056] then, the front face of the insulator layer 22 including the interior of the connection hole 23 -- for example, barrier, such as titanium nitride, -- a conductor -- film 24a -- parallel monotonous mold magnetron sputtering system Endura, for example, AMAT, It deposits by the sputtering method using HP. It turned out that relation (it is a source from the 1996 spring Japan Society of Applied Physics (Toshiba data)) between the amounts Qbd (C/cm2) of charges in case the temperature and gate oxide of the semi-conductor substrate 1 break as shown in drawing 15 is, and the amount of charges in case gate oxide 9 breaks with the rise of the temperature of the semi-conductor substrate 1 also becomes small. that is, -- since it becomes easy to destroy gate oxide 9 with the rise of the temperature of the semi-conductor substrate 1 -- the barrier -- a conductor -- in case film 24a is deposited, temperature of the semi-conductor substrate 1 is made into about 100 degrees C or less (1st sputtering process). In addition, Tox in drawing 15 is the thickness of gate oxide 9. moreover -- since it may happen in the gestalt 3 of this operation that destruction of the gate oxide 9 by the charge-up damage may take place at the moment of beginning to form membranes by the sputtering method on the front face of the insulator layer 22 including the interior of the connection hole 23 -- the barrier -- a conductor -- the thickness of film 24a may be about 5nm.

[0057] next, the barrier -- a conductor -- the front face of film 24a -- for example, barrier, such as titanium nitride, -- a conductor -- film 24b -- about 45nm -- depositing -- the barrier -- a conductor -- film 24a and the barrier -- a conductor -- the barrier whose thickness film 24b is doubled and is about 50nm -- a conductor -- it considers as the film 24. the barrier -- a conductor -- deposition of film 24b -- parallel monotonous mold magnetron sputtering system Endura, for example, AMAT, the sputtering method using HP -- using -- the temperature of the semi-conductor substrate 1 in that case -- the barrier -- a conductor -- it may be higher than the temperature of the semi-conductor substrate 1 when depositing film 24a (2nd sputtering process).

[0058] Then, after forming a plug 26 at the process explained using drawing 7 and drawing 8 in the gestalt 1 of said operation, and the same process, the conductive film 27, such as titanium nitride, is deposited by the sputtering method all over the semi-conductor substrate 1. this time

-- the gestalt 3 of this about 5nm operation of the beginning of the conductive film 27 -- setting -- the barrier -- a conductor -- it can prevent the gate oxide 9 by the charge-up rise damage breaking by depositing on the same conditions as the conditions when depositing film 24a. moreover, all the conductive film 27 -- the barrier -- a conductor -- you may deposit on the same conditions as the conditions when depositing film 24a.

[0059] Then, wiring 30 is formed by depositing and carrying out patterning of the conductive film 28 and the conductive film 29 at the process explained using drawing 9 and drawing 10 in the gestalt 1 of said operation, and the same process.

[0060] Then, after forming an insulator layer 31 and the connection hole 32 at the process explained using drawing 11 in the gestalt 1 of said operation, and the same process, according to the plug 26 explained in the gestalt 3 of this operation, and the formation process of wiring 30 and the same process, a plug 33 and wiring 34 are formed,and the semiconductor integrated circuit equipment of the gestalt 3 of this operation is manufactured.

[0061] As mentioned above, although invention made by this invention person was concretely explained based on the gestalt of implementation of invention, it cannot be overemphasized that it can change variously in the range which this invention is not limited to the gestalt of said operation, and does not deviate from the summary.

[0062] For example, in the gestalt 1 of operation, although Salicide was performed using the titanium film and the titanium silicide film was formed, a silicide-ized reaction may be produced using the tungsten film, the molybdenum film, the tantalum film, or the cobalt film.

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the important section sectional view having shown an example of the manufacture approach of the semiconductor integrated circuit equipment which is the gestalt of 1 operation of this invention.
[Drawing 2] It is an important section sectional view in the production process of the semiconductor integrated circuit equipment following drawing 1 .
[Drawing 3] It is the explanatory view of a collimation sputtering system.
[Drawing 4] It is the explanatory view of a long slow sputtering system.
[Drawing 5] It is the explanatory view showing the distance between the target of a sputtering system, and a semi-conductor substrate, and relation with the rate of gate oxide destruction (defect).
[Drawing 6] It is the explanatory view showing the distance between the target of a sputtering system, and a semi-conductor substrate, and the flow of a plasma electron.
[Drawing 7] It is an important section sectional view in the production process of the semiconductor integrated circuit equipment following drawing 2 .
[Drawing 8] It is an important section sectional view in the production process of the semiconductor integrated circuit equipment following drawing 7 .
[Drawing 9] It is an important section sectional view in the production process of the semiconductor integrated circuit equipment following drawing 8 .
[Drawing 10] It is an important section sectional view in the production process of the semiconductor integrated circuit equipment following drawing 9 .
[Drawing 11] It is an important section sectional view in the production process of the semiconductor integrated circuit equipment following drawing 10 .
[Drawing 12] It is the important section sectional view having shown an example of the manufacture approach of the semiconductor integrated circuit equipment which is the gestalt of other operations of this invention.
[Drawing 13] It is the explanatory view showing the relation between the pressure of the argon gas of a sputtering system, and the rate of gate oxide destruction (defect).
[Drawing 14] It is an important section sectional view in the production process of the semiconductor integrated circuit equipment following drawing 12 .
[Drawing 15] It is the explanatory view showing relation with the amount of charges in case the temperature and gate oxide of a semi-conductor substrate break.
[Description of Notations]
1 Semi-conductor Substrate
4 Isolation Slot
5 Silicon Oxide Film
6 Silicon Oxide Film
7 P Mold Well
8 It is Well N Molds.
9 Gate Oxide
15n Gate electrode

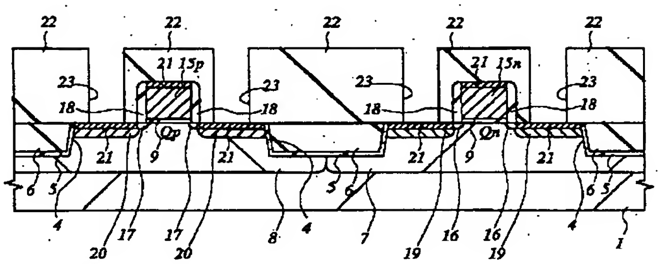
15p Gate electrode
16 N-Mold Semiconductor Region (Source, Drain)
17 P-Mold Semiconductor Region (Source, Drain)
18 Sidewall Spacer
19 N+ Mold Semiconductor Region (Source, Drain)
20 P+ Mold Semiconductor Region (Source, Drain)
21 Titanium Silicide Film 22 Insulator Layer
23 Connection Hole
24 Barrier -- Conductor -- Film (1st Conductivity Film)
24a the barrier -- a conductor -- the film
24b the barrier -- a conductor -- the film
25 Conductive Film (2nd Conductivity Film)
26 Plug
27 Conductive Film
28 Conductive Film
29 Conductive Film
30 Wiring
31 Insulator Layer
32 Connection Hole
33 Plug
34 Wiring
Qn N channel mold MISFET
Qp P channel mold MISFET

[Translation done.]

DRAWINGS

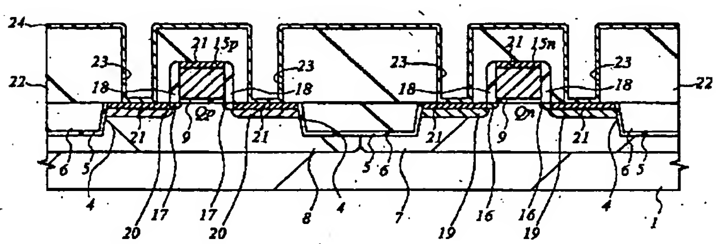
[Drawing 1]

図 1



[Drawing 2]

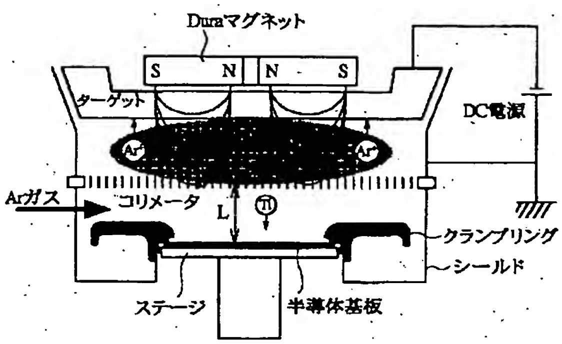
図 2



1：半導体基板
22：絶縁膜
23：接続孔
24：バリア導体膜

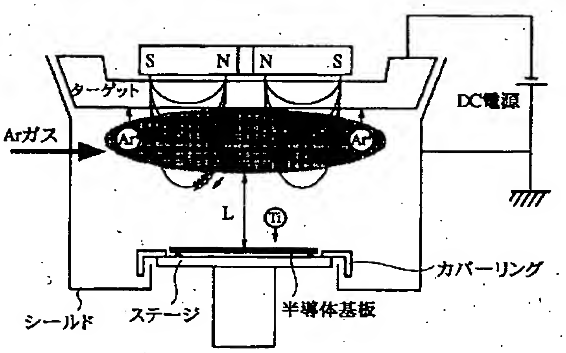
[Drawing 3]

図 3



[Drawing 4]

図 4



[Drawing 5]

図 5

<table>
<tr><th>ターゲット-半導体基板間距離</th><th>52mm（標準）</th><th>62mm</th></tr>
<tr><td>結果</td><td>
[V]
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[V]
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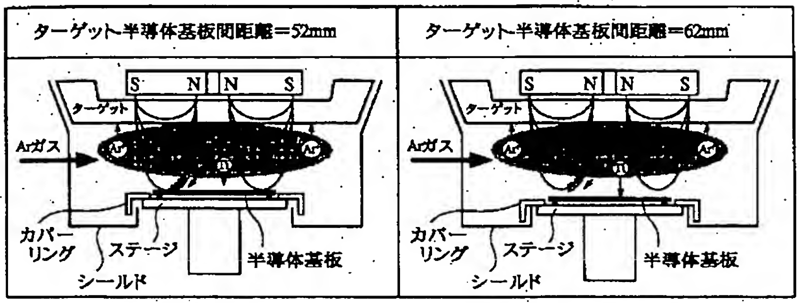
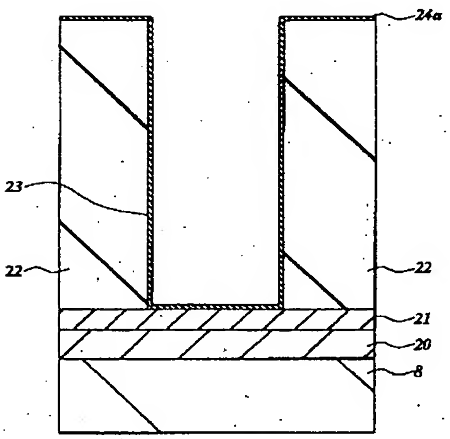
[Drawing 6]

図 6



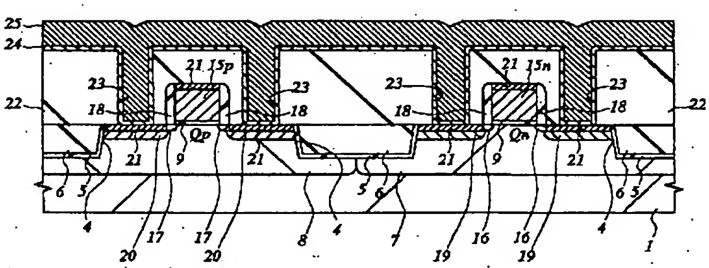
[Drawing 12]

図 12



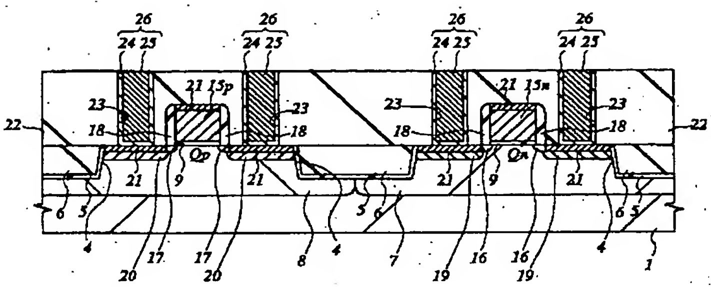
[Drawing 7]

図 7



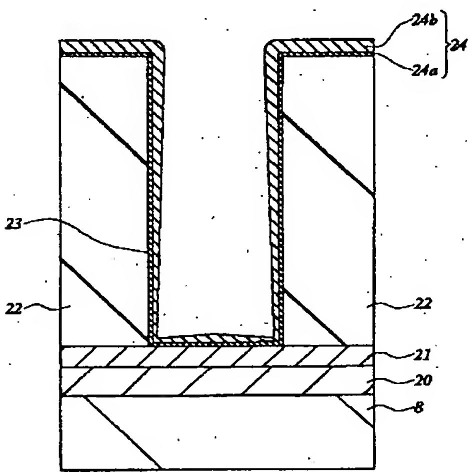
[Drawing 8]

図 8



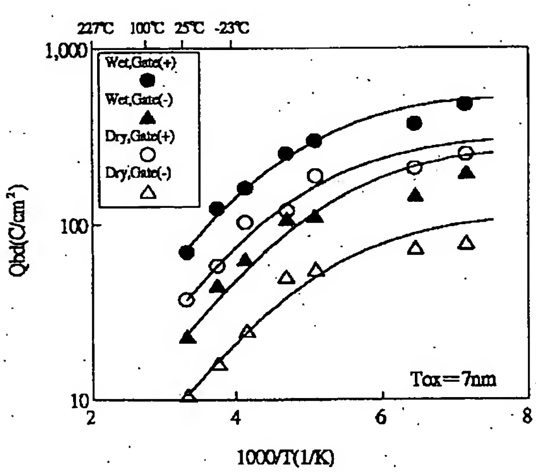
[Drawing 14]

図 14



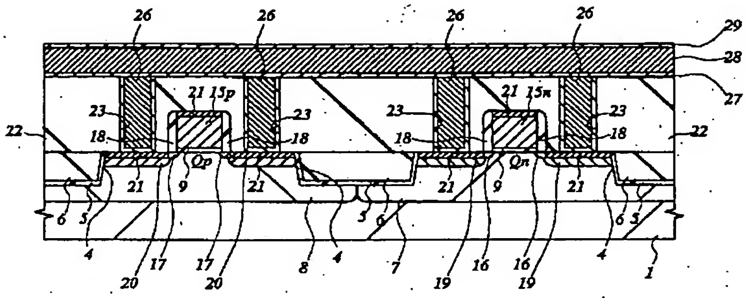
[Drawing 15]

図 15



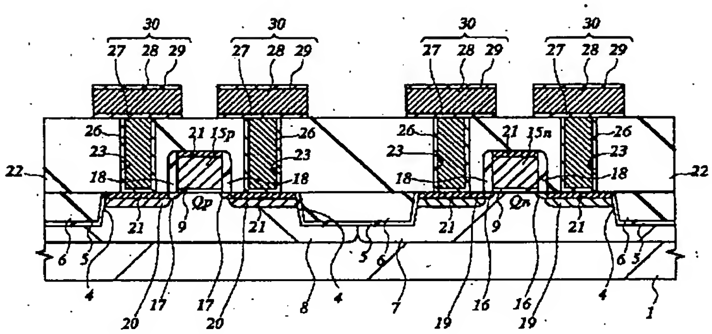
[Drawing 9]

図 9



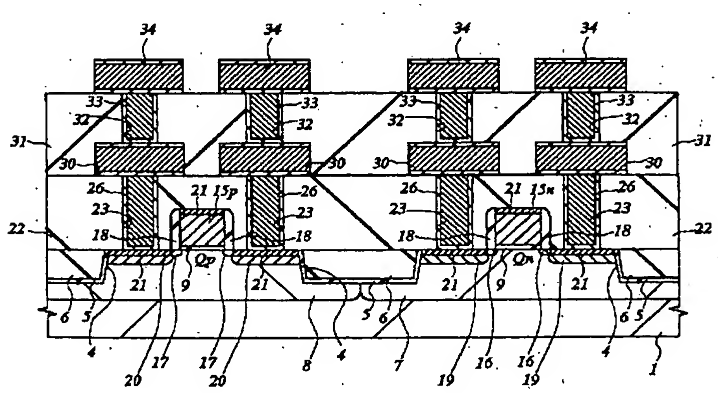
[Drawing 10]

図 10



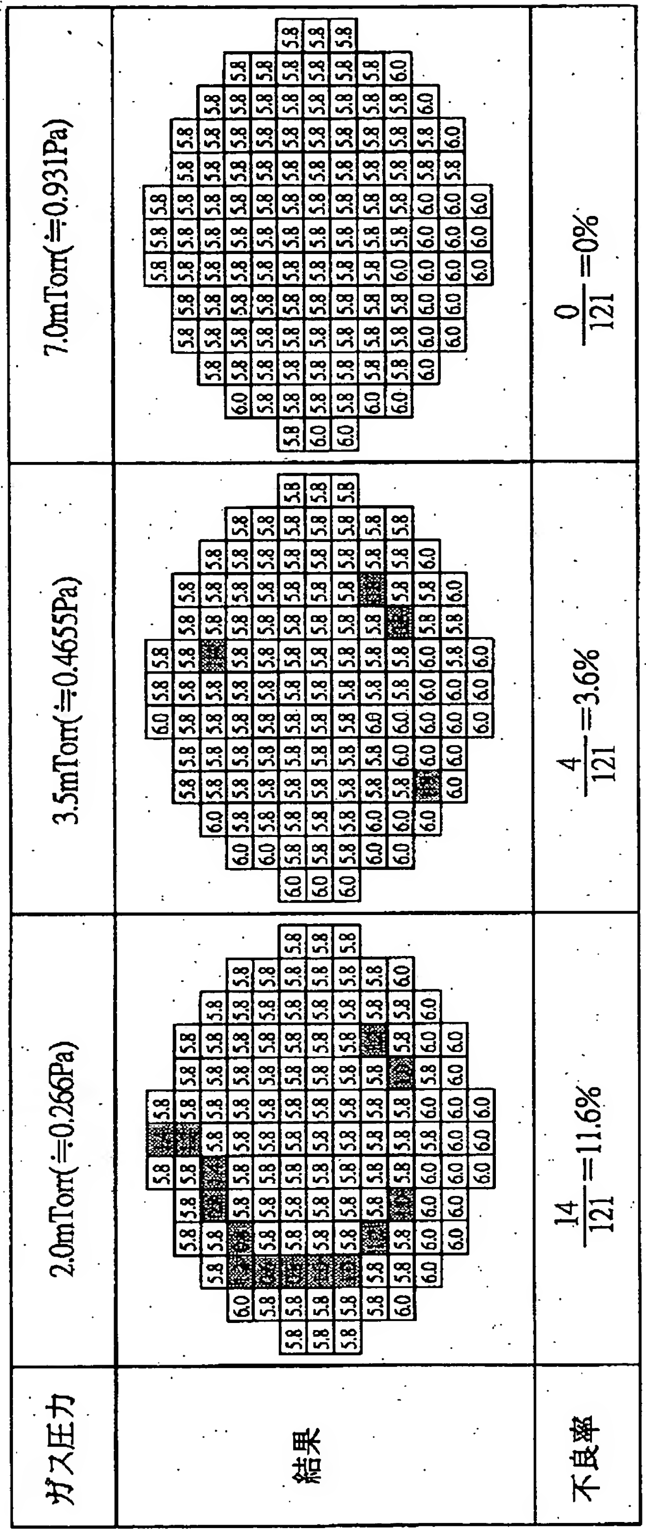
[Drawing 11]

図 11



[Drawing 13]

図 13



[Translation done.]

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21/8238			27/08	321F	5F048
27/092			29/78	301F	5F103

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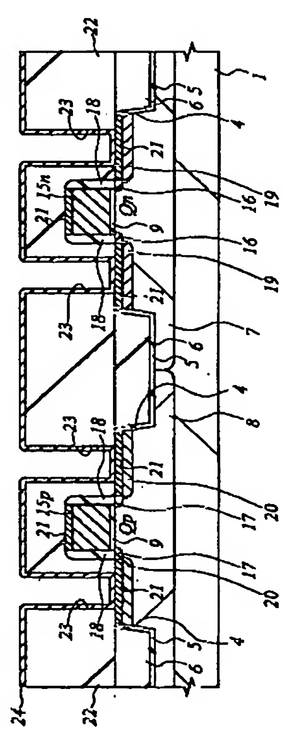
(54)【発明の名称】　半導体集積回路装置の製造方法

(57)【要約】
【課題】　スパッタリング法にて薄膜を堆積する際に発生するプラズマ電子の半導体基板への流入を低減し、チャージアップダメージによるゲート酸化膜の破壊を防ぐ
【解決手段】　絶縁膜２２に接続孔２３が形成され、接続孔２３の内部を含む絶縁膜２２の表面にスパッタリング法にてバリア導体膜２４を堆積する工程において、バリア導体膜２４の堆積にはプラズマ電子の半導体基板１への流入を低減する手法を用いる。プラズマ電子の半導体基板１への流入を低減する手法として、たとえばコリメーションスパッタリング装置またはロングスロースパッタリング装置を用いる。

図２



1：半導体基板
22：絶縁膜
23：接続孔
24：バリア導体膜

【特許請求の範囲】

【請求項１】　半導体基板の主面上に堆積された絶縁膜の表面に接続孔を開孔後、導電性膜を堆積する際に、第１および第２のスパッタリング工程を順に含み、前記第１のスパッタリング工程はスパッタリングにおいて発生する電子の前記半導体基板への流入を抑制するスパッタリング法であることを特徴とする半導体集積回路装置の製造方法。

【請求項２】　（ａ）半導体基板の主面上に堆積された絶縁膜の表面に接続孔を開孔後、第１導電性膜をスパッタリング法にて堆積する工程、（ｂ）前記第１導電性膜の表面に第２導電性膜を堆積する工程、を含み、前記第１導電性膜は、スパッタリングにおいて発生する電子の前記半導体基板への流入を抑制するスパッタリング条件にて堆積することを特徴とする半導体集積回路装置の製造方法。

【請求項３】　（ａ）半導体基板の主面上に堆積された絶縁膜の表面に接続孔を開孔後、第１導電性膜をスパッタリング法にて堆積する工程、（ｂ）前記第１導電性膜の表面に第２導電性膜を堆積する工程、を含み、前記第１導電性膜はコリメーションスパッタリング法、ロングスロースパッタリング法またはスパッタリングにおいて発生する電子が前記半導体基板へ流入することを抑制または防止する放電ガス圧力条件としたスパッタリング法にて堆積することを特徴とする半導体集積回路装置の製造方法。

【請求項４】　（ａ）半導体基板の主面上に堆積された絶縁膜にプラグを形成した後、前記プラグを含む前記絶縁膜の表面に導電性膜を堆積する際に、第１および第２のスパッタリング工程を順に含み、前記第１のスパッタリング工程はスパッタリングにおいて発生する電子の前記半導体基板への流入を抑制するスパッタリング法であることを特徴とする半導体集積回路装置の製造方法。

【請求項５】　（ａ）半導体基板の主面上に堆積された絶縁膜にプラグを形成した後、前記プラグを含む前記絶縁膜の表面に第１導電性膜をスパッタリング法にて堆積する工程、（ｂ）前記第１導電性膜の表面に第２導電性膜を堆積する工程、を含み、前記第１導電性膜は、スパッタリングにおいて発生する電子の前記半導体基板への流入を抑制するスパッタリング条件にて堆積することを特徴とする半導体集積回路装置の製造方法。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、半導体集積回路装置の製造技術に関し、特に、プラズマを使用したスパッタリング法によって薄膜が堆積される半導体集積回路装置の製造技術に適用して有効な技術に関するものである。

【０００２】

【従来の技術】ＭＩＳＦＥＴ（Metal Insulator Semiconductor Field Effect Transistor）を有する半導体集積回路装置の薄膜形成プロセスにおいては、たとえば、１９９１年１１月２２日、株式会社工業調査会発行の「１９９２年版超ＬＳＩ製造・試験装置ガイドブック」、ｐ８４〜ｐ９３に記載されているように、スパッタリング法にて行われる成膜についてのほとんどは、薄膜形成の高速化のためにマグネトロンスパッタ法が用いられてきた。

【０００３】現在のマグネトロンスパッタ法は、主に比較的低いガス圧でプラズマが発生し、成膜できるようなシステムのものが主流であり、（ａ）低電圧および大電流の理想的な放電特性が得られるので、消費電力当たりのスパッタリング効率が向上する、（ｂ）スパッタされる原子は対向して配置されている半導体基板に効率よく到達するので、高速での成膜が可能である、（ｃ）半導体基板への電子の衝突を減らせるため、半導体基板の温度の上昇を低減し、低温での成膜が可能である、等の特徴を有する。

【０００４】

【発明が解決しようとする課題】ところが、本発明者らは、プラズマ装置を用いるマグネトロンスパッタリング法にて薄膜を堆積する従来の技術においては、以下のような問題を生ずることを見出した。

【０００５】すなわち、プラズマ中の電子は、マグネットの磁場に沿うように半導体基板上に流入する。この流入した電子が半導体基板に蓄積され、半導体基板の電子が流入する部分とその他の部分で電位差が生じる。この電位差に起因する電流（ダメージ電流）が半導体基板を流れることにより、半導体基板の主面上に形成されたＭＩＳＦＥＴのゲート酸化膜が破壊または劣化する場合がある。そのため、プラズマを使用するスパッタ装置に対して対策を施す必要があり、電子の半導体基板への流入を阻害するスパッタチャンバやプロセスを用いる必要がある。

【０００６】本発明の目的は、ＭＩＳＦＥＴのゲート酸化膜を破壊または劣化することなくプラズマを用いたスパッタリング法にて薄膜を堆積する技術を提供することにある。

【０００７】本発明の前記ならびにその他の目的と新規な特徴は、本明細書の記述および添付図面から明らかになるであろう。

【０００８】

【課題を解決するための手段】本願において開示される発明のうち、代表的なものの概要を簡単に説明すれば、次のとおりである。

【０００９】すなわち、本発明は、半導体基板の主面上に堆積された絶縁膜の表面に接続孔を開孔後、導電性膜を堆積する際に、第１および第２のスパッタリング工程を順に含み、前記第１のスパッタリング工程はスパッタリングにおいて発生する電子の前記半導体基板への流入

を抑制するスパッタリング法である。

【0010】また、本発明は、半導体基板の主面上に堆積された絶縁膜の表面に接続孔を開孔後、第1導電性膜をスパッタリング法にて堆積する工程と、前記第1導電性膜の表面に主導電層となる第2導電性膜を堆積する工程とを含むものであり、前記第1導電性膜は、スパッタリングにおいて発生する電子の前記半導体基板への流入を抑制するスパッタリング条件にて堆積するものである。

【0011】また、本発明は、半導体基板の主面上に堆積された絶縁膜の表面に接続孔を開孔後、第1導電性膜をスパッタリング法にて堆積する工程と、前記第1導電性膜の表面に主導電層となる第2導電性膜を堆積する工程とを含むものであり、前記第1導電性膜はコリメーションスパッタリング法にて堆積するものである。

【0012】また、本発明は、半導体基板の主面上に堆積された絶縁膜の表面に接続孔を開孔後、第1導電性膜をスパッタリング法にて堆積する工程と、前記第1導電性膜の表面に主導電層となる第2導電性膜を堆積する工程とを含むものであり、前記第1導電性膜はロングスロースパッタリング法にて堆積するものである。

【0013】また、本発明は、半導体基板の主面上に堆積された絶縁膜の表面に接続孔を開孔後、第1導電性膜をスパッタリング法にて堆積する工程と、前記第1導電性膜の表面に主導電層となる第2導電性膜を堆積する工程とを含むものであり、前記第1導電性膜は、スパッタリングにおいて発生する電子が前記半導体基板へ流入することを防ぐために、プラズマ電子が半導体基板に到達するまでにアルゴンガスと少なくとも4回以上衝突する放電ガス圧力のスパッタリング法にて堆積するものである。

【0014】また、本発明は、半導体基板の主面上に堆積された絶縁膜の表面に接続孔を開孔後、第1導電性膜をスパッタリング法にて堆積する工程と、前記第1導電性膜の表面に主導電層となる第2導電性膜を堆積する工程とを含むものであり、前記第1導電性膜は、前記半導体基板の温度を100℃以下とした条件下でのスパッタリング法にて堆積するものである。

【0015】また、本発明は、半導体基板の主面上に堆積された絶縁膜にプラグを形成した後、前記プラグを含む前記絶縁膜の表面に導電性膜を堆積する際に、第1および第2のスパッタリング工程を順に含み、前記第1のスパッタリング工程はスパッタリングにおいて発生する電子の前記半導体基板への流入を抑制するスパッタリング法である。

【0016】また、本発明は、半導体基板の主面上に堆積された絶縁膜にプラグを形成した後、前記プラグを含む前記絶縁膜の表面に第1導電性膜をスパッタリング法にて堆積する工程と、前記第1導電性膜の表面に主導電層となる第2導電性膜を堆積する工程とを含むものであり、前記第1導電性膜は、スパッタリングにおいて発生する電子の前記半導体基板への流入を抑制するスパッタリング条件にて堆積するものである。

【0017】上記の本発明によれば、接続孔を含む絶縁膜上に導電性膜を第1のスパッタリング工程にて堆積する際に、スパッタリング時に発生するプラズマ電子が接続孔を通してゲート電極へ流入することを防ぐことができるので、半導体基板の電子が流入する部分とその他の部分で電位差が生じることを防ぐことができる。その結果、前記電位差に起因する電流（チャージアップダメージ電流）が前記半導体基板を流れることを防ぐことができるので、前記半導体基板の主面上に形成されたMISFETのゲート酸化膜の破壊または劣化を防ぎ、半導体集積回路装置の歩留まりおよび信頼性を向上させることができる。

【0018】また、上記の本発明によれば、接続孔を含む絶縁膜上に第1導電性膜をスパッタリング法を用いて堆積する際に、プラズマ電子が半導体基板に到達するまでにアルゴン原子と少なくとも4回以上衝突する放電ガス圧力とすることで、プラズマ電子を前記半導体基板まで到達しにくくすることができる。その結果、プラズマ電子が接続孔を通してゲート電極へ流入することを防ぐことができるので、チャージアップダメージ電流が流れることに起因するMISFETのゲート酸化膜の破壊または劣化を防ぎ、半導体集積回路装置の歩留まりおよび信頼性を向上させることができる。

【0019】また、上記の本発明によれば、半導体基板の温度を100℃以下とした条件下で接続孔を含む絶縁膜上に第1導電性膜をスパッタリング法を用いて堆積するので、MISFETのゲート酸化膜が破壊する時の電荷量値を向上できる。その結果、チャージアップダメージ電流に起因する前記ゲート酸化膜の破壊または劣化を防ぎ、半導体集積回路装置の歩留まりおよび信頼性を向上させることができる。

【0020】

【発明の実施の形態】以下、本発明の実施の形態を図面に基づいて詳細に説明する。なお、実施の形態を説明するための全図において、同一の機能を有する部材には同一の符号を付し、その繰り返しの説明は省略する。

【0021】（実施の形態1）本実施の形態1は、nチャネル型MISFETQnとpチャネル型MISFETQpとで構成した半導体集積回路装置の製造方法に本発明を適用したものである。

【0022】以下、上記した半導体集積回路装置の製造方法を図1～図9を用いて工程順に説明する。

【0023】まず、図1に示すように、比抵抗が10Ωcm程度の単結晶シリコンからなる半導体基板1を850℃程度で熱処理して、その主面に膜厚10nm程度の薄い酸化シリコン膜（パッド酸化膜）を形成し、次いでこの酸化シリコン膜の上に膜厚120nm程度の窒化シ

リコン膜をCVD（Chemical Vapor Deposition）法で堆積した後、フォトレジスト膜をマスクにしたドライエッチングで素子分離領域の窒化シリコン膜と酸化シリコン膜とを除去する。酸化シリコン膜は、後の工程で素子分離溝の内部に埋め込まれる酸化シリコン膜をデンシファイ（焼き締め）するときなどに基板に加わるストレスを緩和する目的で形成される。また、窒化シリコン膜は酸化されにくい性質を持つので、その下部（活性領域）の基板表面の酸化を防止するマスクとして利用される。

【００２４】続いて、窒化シリコン膜をマスクにしたドライエッチングで素子分離領域の半導体基板１に深さ３５０ｎｍ程度の溝を形成した後、エッチングで溝の内壁に生じたダメージ層を除去するために、半導体基板１を１０００℃程度で熱処理して溝の内壁に膜厚１０ｎｍ程度の薄い酸化シリコン膜５を形成する。

【００２５】続いて、半導体基板１上に膜厚３８０ｎｍ程度の酸化シリコン膜６をCVD法で堆積し、次いで酸化シリコン膜６の膜質を改善するために、半導体基板１を熱処理して酸化シリコン膜６をデンシファイ（焼締め）する。その後、窒化シリコン膜をストッパに用いた化学的機械研磨（Chemical Mechanical Polishing；CMP）法で酸化シリコン膜６を研磨して溝の内部に残すことにより、表面が平坦化された素子分離溝４を形成する。

【００２６】続いて、熱リン酸を用いたウェットエッチングで半導体基板１の活性領域上に残った窒化シリコン膜を除去した後、半導体基板１のｎチャネル型ＭＩＳＦＥＴを形成する領域にＢ（ホウ素）をイオン注入してｐ型ウエル７を形成し、ｐチャネル型ＭＩＳＦＥＴを形成する領域にＰ（リン）をイオン注入してｎ型ウエル８を形成する。

【００２７】続いて、ｐ型ウエル７およびｎ型ウエル８のそれぞれの表面の酸化シリコン膜をＨＦ（フッ酸）系の洗浄液を使って除去した後、半導体基板１をウェット酸化してｐ型ウエル７およびｎ型ウエル８のそれぞれの表面に膜厚３．５ｎｍ程度の清浄なゲート酸化膜９を形成する。

【００２８】次に、半導体基板１上に膜厚９０～１００ｎｍ程度のノンドープ多結晶シリコン膜をCVD法で堆積する。続いて、イオン注入用のマスクを用いて、ｐ型ウエル７の上部のノンドープ多結晶シリコン膜にＰ（リン）をイオン注入してｎ型多結晶シリコン膜を形成する。さらに続いて、イオン注入用のマスクを用いて、ｎ型ウエル８のノンドープ多結晶シリコン膜にＢ（ホウ素）をイオン注入してｐ型多結晶シリコン膜を形成する。

【００２９】次に、フォトレジスト膜をマスクにしてｎ型多結晶シリコン膜およびｐ型多結晶シリコン膜をドライエッチングする。これにより、ｐ型ウエル７のゲート酸化膜９の上部にｎ型多結晶シリコンからなるｎチャネル型ＭＩＳＦＥＴのゲート電極１５ｎが形成され、ｎ型ウエル８のゲート酸化膜９の上部にｐ型多結晶シリコン膜からなるｐチャネル型ＭＩＳＦＥＴのゲート電極１５ｐが形成される。ゲート電極１５ｎおよびゲート電極１５ｐのゲート長は、たとえば０．２５μｍである。

【００３０】次に、ゲート電極１５ｎおよび１５ｐの加工に用いたフォトレジスト膜を除去した後、ｐ型ウエル７にｎ型不純物、例えばＰ（リン）をイオン注入してゲート電極１５ｎの両側のｐ型ウエル７にn^-型半導体領域１６を形成し、ｎ型ウエル８にｐ型不純物、例えばＢ（ホウ素）をイオン注入してゲート電極１５ｐの両側のｎ型ウエル８にp^-型半導体領域１７を形成する。

【００３１】次に、半導体基板１上に膜厚１００ｎｍ程度の酸化シリコン膜をCVD法で堆積し、反応性イオンエッチング（ＲＩＥ）法を用いてこの酸化シリコン膜を異方性エッチングすることにより、ｎチャネル型ＭＩＳＦＥＴのゲート電極１５ｎおよびｐチャネル型ＭＩＳＦＥＴのゲート電極１５ｐのそれぞれの側壁にサイドウォールスペーサ１８を形成する。続いて、ｐ型ウエル７にｎ型不純物、例えばＡｓ（ヒ素）をイオン注入してｎチャネル型ＭＩＳＦＥＴのn^+型半導体領域１９（ソース、ドレイン）を形成し、ｎ型ウエル８にｐ型不純物、例えばＢ（ホウ素）をイオン注入してｐチャネル型ＭＩＳＦＥＴのp^+型半導体領域２０（ソース、ドレイン）を形成する。これにより、ｎチャネル型ＭＩＳＦＥＴおよびｐチャネル型ＭＩＳＦＥＴのそれぞれにＬＤＤ（Lightly Doped Drain）構造のソース、ドレイン領域が形成され、ｎチャネル型ＭＩＳＦＥＴＱｎおよびｐチャネル型ＭＩＳＦＥＴＱｐが完成する。

【００３２】次に、スパッタリング法を用いて半導体基板１の全面にチタン膜を堆積する。続いて、半導体基板１を窒素ガス雰囲気中、６５０～７００℃程度の温度でアニール（第1アニール）することにより、ゲート電極１５ｎおよび１５ｐとチタン膜との界面、およびソース、ドレイン領域（n^+半導体領域１９、p^+半導体領域２０）と前記チタン膜との界面にシリサイド化反応を生じさせてチタンシリサイド膜２１を形成する。

【００３３】次に、半導体基板１上にCVD法で酸化シリコン膜を堆積し、CMP法を用いてその表面を平坦化することにより絶縁膜２２を形成する。さらに、絶縁膜２２にフォトリソグラフィ技術を用いて接続孔２３を開孔する。

【００３４】続いて、接続孔２３の内部を含む絶縁膜２２の表面をスパッタエッチングし、接続孔２３の内部を含む絶縁膜２２の表面の表面に形成された自然酸化膜を除去する。このスパッタエッチングにより、後の工程において接続孔２３の内部に形成されるプラグ２６と、接続孔２３の底部のチタンシリサイド膜２１との間の電気的抵抗が低減される。

【００３５】次に、図２に示すように、接続孔２３の内

部を含む絶縁膜２２の表面に、膜厚が約５０ｎｍ程度の、たとえば窒化チタンなどのバリア導体膜（第１導電性膜）２４を堆積する。このバリア導体膜２４の堆積に一般的な平行平板型のスパッタリング装置を用いると、ターゲットと半導体基板との間の距離が小さいため、スパッタリング時に発生するプラズマ電子が接続孔２３を通してチタンシリサイド膜２１へ流入し、半導体基板１の電子が流入する部分とその他の部分で電位差が生じる。その結果、その電位差に起因する電流（チャージアップダメージ電流）が半導体基板１を流れ、ゲート酸化膜９の破壊または劣化が発生する場合がある。そこで、本実施の形態１においては、図３に示すコリメーションスパッタリング装置、または図４に示すロングスロースパッタリング装置を用いてバリア導体膜２４の堆積を行う。コリメーションスパッタリング装置およびロングスロースパッタリング装置は、ターゲットと半導体基板１との間の距離が、一般的な平行平板型のスパッタリング装置と比べて大きくなり、装置内のプラズマ中の電子の半導体基板上への流入を減少させることができるので、接続孔２３を通してプラズマ電子によってチタンシリサイド膜２１が帯電することを防ぎ、チャージアップダメージ電流によるゲート酸化膜９の破壊または劣化を防ぐことができる。

【００３６】また、接続孔２３を通してチタンシリサイド膜２１へプラズマ電子が流入し、チャージアップダメージによるゲート酸化膜９の破壊が起こり得るのはバリア導体膜２４が堆積し始める瞬間である。バリア導体膜２４がある程度堆積された後は、プラズマ電子は半導体基板１の面内の電位差を打ち消すように堆積した半導体基板１の表面の膜中を移動し、ゲート電極１５ｎおよび１５ｐには帯電しない。そのため、チャージアップダメージによるゲート酸化膜９の破壊を防ぐことができるので、後の工程で形成される導電性膜２５、２８および２９の堆積に用いるスパッタリング法は、コリメーションスパッタリングまたはロングスロースパッタリングに限定するものではない。

【００３７】本発明者らが、スパッタリング時のターゲットと半導体基板との間の距離と、ゲート酸化膜破壊の発生率（不良率）との関係を実験により調査したところ、図５に示すように、ターゲットと半導体基板との間の距離が大きくなるほど、ゲート酸化膜破壊の発生率（不良率）が低くなることが定量的に判断できるようになった。たとえば、図６に示すように、ターゲットと半導体基板の間の距離が５２ｍｍの時には、プラズマ中の電子がマグネットの磁場に沿うように半導体基板上に流入してしまうが、ターゲットと半導体基板の間の距離が６２ｍｍの時には、ターゲットと半導体基板の間の距離が伸びたことにより、半導体基板が設置されている位置ではマグネットの磁場の影響が小さくなり、プラズマ中の電子の半導体基板上への流入を減少させることができる。本実施の形態１において、コリメーションスパッタリング装置またはロングスロースパッタリング装置のチャンバ内におけるプラズマと半導体基板の間の距離Ｌは、たとえば約１０ｃｍ程度である。そのため、チャージアップダメージの原因となる電子の半導体基板１への流入をＬが６２ｍｍの時よりもさらに低減することが可能となり、Ｌが６２ｍｍの時よりもさらにチャージアップアップダメージによるゲート酸化膜９の破壊を抑制または防止することができる。

【００３８】なお、コリメーションスパッタリングは、本来は、ターゲットと半導体基板の間に穴のあいた円盤を入れ、スパッタされた粒子の斜め成分をカットし指向性を上げる手法である。また、ロングスロースパッタリングは、本来は、スパッタされた粒子の垂直方向の成分を半導体基板に堆積するように、ターゲットと半導体基板の間の距離を延ばすことで指向性を上げる手法である。

【００３９】次に、図７に示すように、前記バリア導体膜２４の表面に前記接続孔２３の内部を埋め込む、たとえばタングステンなどの導電性膜（第２導電性膜）２５を堆積する。この導電性膜２５の堆積は、たとえばＷ−ＣＶＤ法（装置：たとえばＡＭＡＴ社Ｃｅｎｔｕｒａ−Ｗ）により行う。

【００４０】次に、図８に示すように、接続孔２３以外の絶縁膜２２上のバリア導体膜２４および導電性膜２５を、たとえばＣＭＰ法により除去しプラグ２６を形成する。

【００４１】次に、図９に示すように、半導体基板１の全面に、コリメーションスパッタリング装置またはロングスロースパッタリング装置を用いて、たとえば窒化チタンなどの導電性膜（第１導電性膜）２７を堆積する。導電性膜２７は、コリメーションスパッタリング装置またはロングスロースパッタリング装置によって堆積するため、プラグ２６へプラズマ電子が流入することを防ぐことができ、チャージアップダメージの原因となる電子の半導体基板１への流入を低減することが可能となるので、チャージアップアップダメージによるゲート酸化膜９が破壊することを防ぐことができる。

【００４２】続いて、導電性膜２７の表面に、たとえばアルミニウムなどの導電性膜（第２導電性膜）２８を堆積する。さらに続けて、その導電性膜２８の表面に、たとえば窒化チタンなどの導電性膜２９を堆積する。この導電性膜２９は、導電性膜２７、導電性膜２８および導電性膜２９をフォトリソグラフィ工程によりパターニングする際に、光の乱反射を防ぐ機能を有する。導電性膜２８および導電性膜２９の堆積は、コリメーションスパッタリング装置およびロングスロースパッタリング装置以外の平行平板型マグネトロンスパッタリング装置、たとえばＡＭＡＴ社Ｅｎｄｕｒａ　ＨＰを用いたスパッタリング法にて行う。

【0043】次に、図10に示すように、導電性膜27、導電性膜28および導電性膜29をドライエッチング技術を用いて加工し、配線30を形成する。

【0044】次に、図11に示すように、図1〜図10を用いて説明した工程と同様の工程により、絶縁膜31、接続孔32、プラグ33および配線34を形成して、本実施の形態1の半導体集積回路装置を製造する。なお、配線34の上部に、さらに多層に配線を形成してもよい。

【0045】本実施の形態1の半導体集積回路装置の製造方法によれば、チャージアップアップダメージによる前記ゲート酸化膜9の破壊を防ぐことができるので、半導体集積回路装置の歩留まりおよび信頼性を向上することができる。

【0046】(実施の形態2)本実施の形態2の半導体集積回路装置の製造方法は、前記実施の形態1におけるバリア導体膜24および導電性膜27の堆積処理に際し、別の低ダメージ条件のスパッタリング法を用いたものである。その他の工程および部材は前記実施の形態1と同様であるので、それら同様の工程および部材についての説明は省略する。

【0047】本実施の形態2の半導体集積回路装置の製造方法を図12〜図14を用いて説明する。

【0048】本実施の形態2の半導体集積回路装置の製造方法は、前記実施の形態1において図1を用いて説明した工程までは同様である。

【0049】その後、接続孔23付近を拡大した図12に示すように、接続孔23の内部を含む絶縁膜22の表面に、たとえば窒化チタンなどのバリア導体膜24aを堆積する。このバリア導体膜24aは、ターゲットと半導体基板1との間の距離(T/S)が約5cm程度となるチャンバを有するスパッタリング装置で堆積する(第1のスパッタリング工程)。本発明者らは、T/S=5cmの時に、ゲート酸化膜9を破壊しないスパッタリング時のアルゴンガスの圧力を実験により調査した。その結果、図13に示すように、アルゴンガスの圧力を約7mTorr(≒0.931Pa)以上とする時に、プラズマ電子は半導体基板1に到達するまでにアルゴン原子と衝突を繰り返して融和するために、半導体基板1まで届きにくくなり、チタンシリサイド膜21へ流入しにくくなるので、チャージアップダメージによるゲート酸化膜9の破壊が発生しないことが明らかになった。この時、チャンバ内のプラズマ中の電子が、半導体基板に到達するまでにアルゴンと衝突する回数をc(回)とすれば、$c=L/\lambda$で表される。ここで、$L=T/S$(cm)であり、λは電子の平均自由行程であり、$\lambda=10^{-2}/P$(cm)で表される。Pはアルゴンガスの圧力(単位はTorr)である。本発明者の調査によると、T/S=5cmの場合、Pが約7mTorr(≒0.931Pa)以上となる条件においてゲート酸化膜は破壊されないのであるから、cは計算上3.5回となり、実際にはcが4回以上となるPでバリア導体膜24aを堆積すればよい。本実施の形態2においては、バリア導体膜24aを堆積する際のPは、たとえば約8mTorr(≒1.064Pa)とする。また、前記実施の形態1において、バリア導体膜24を堆積する工程のところで述べた理由と同様の理由により、チャージアップダメージによるゲート酸化膜9の破壊が起こり得るのは、接続孔23の内部を含む絶縁膜22の表面にスパッタリング法にて成膜し始める瞬間である。本実施の形態2においては、バリア導体膜24aの膜厚は、たとえばバリア導体膜24aの膜厚と後述するバリア導体膜24bの膜厚との合計値の約1/10程度とするものであり、その合計値は、約50nm程度であるので、バリア導体膜24aの膜厚は好ましくは約5nm程度とする。なお、T/S=5cm以外の場合においても、cが4回以上となるようにPを設定すればよく、$c=L/\lambda$、$L=T/S$および$\lambda=10^{-2}/P$であることから、$P=c\times10^{-2}/L$とし、cに4を代入し、Lの具体的数値を代入して、Pの最低値を求めることができる。

【0050】次に、図14に示すように、前記バリア導体膜24aの表面に、たとえば窒化チタンなどのバリア導体膜24bを約45nm程度堆積し、前記バリア導体膜24aと前記バリア導体膜24bとを合わせて、膜厚が約50nm程度のバリア導体膜24とする。そのバリア導体膜24bの堆積にはスパッタリング法を用い、前記バリア導体膜24aを堆積したときのアルゴンガス圧力よりも低い圧力で堆積する(第2のスパッタリング工程)が、前記バリア導体膜24aを堆積したときのアルゴンガス圧力と同程度以下の圧力で堆積してもよい。

【0051】その後、前記実施の形態1において図7および図8を用いて説明した工程と同様の工程にてプラグ26を形成し、絶縁膜31を堆積した後、半導体基板1の全面に、たとえば窒化チタンなどの導電性膜27をスパッタリング法にて堆積する。この時、前記導電性膜27の最初の5nm程度は、本実施の形態2において前記バリア導体膜24aを堆積したときの条件と同じ条件にて堆積し、チャージアップアップダメージによる前記ゲート酸化膜9が破壊することを防ぐことができる。また、前記導電性膜27のすべてを前記バリア導体膜24aを堆積したときの条件と同じ条件にて堆積してもよい。

【0052】続いて、前記実施の形態1において図9および図10を用いて説明した工程と同様の工程にて導電性膜28および導電性膜29を堆積し、パターニングすることで配線30を形成する。

【0053】続いて、前記実施の形態1において図11を用いて説明した工程と同様の工程にて絶縁膜31および接続孔32を形成した後、本実施の形態2において説明した前記プラグ26および前記配線30の形成工程と

同様の工程により、プラグ３３および配線３４を形成して、本実施の形態２の半導体集積回路装置を製造する。

【００５４】（実施の形態３）本実施の形態３の半導体集積回路装置の製造方法は、前記実施の形態１または２におけるバリア導体膜２４および導電性膜２７の堆積に、さらに別の低ダメージ条件のスパッタリング法を用いたものである。その他の工程および部材は実施の形態１または２と同様であり、それら同様の工程および部材についての説明は省略する。

【００５５】本実施の形態３の半導体集積回路装置の製造方法を図１５に従って説明する。本実施の形態３の半導体集積回路装置の製造方法は、前記実施の形態１において図１を用いて説明した工程までは同様である。

【００５６】その後、接続孔２３の内部を含む絶縁膜２２の表面に、たとえば窒化チタンなどのバリア導体膜２４ａを平行平板型マグネトロンスパッタリング装置、たとえばＡＭＡＴ社Ｅｎｄｕｒａ　ＨＰを用いたスパッタリング法にて堆積する。半導体基板１の温度とゲート酸化膜が破壊するときの電荷量Q_{bd}（Ｃ／ｃｍ^2）との間には、図１５に示すような関係（１９９６年春季応用物理学会（東芝データ）より出典）があり、半導体基板１の温度の上昇に伴いゲート酸化膜９が破壊するときの電荷量も小さくなることがわかった。つまり、半導体基板１の温度の上昇に伴いゲート酸化膜９は破壊しやすくなるので、バリア導体膜２４ａを堆積する際には、半導体基板１の温度を、たとえば約１００℃以下とする（第１のスパッタリング工程）。なお、図１５中のＴｏｘはゲート酸化膜９の厚さである。また、本実施の形態３において、チャージアップダメージによるゲート酸化膜９の破壊が起こり得るのは、接続孔２３の内部を含む絶縁膜２２の表面にスパッタリング法にて成膜し始める瞬間に起こり得るので、バリア導体膜２４ａの膜厚は、たとえば約５ｎｍ程度とする。

【００５７】次に、バリア導体膜２４ａの表面に、たとえば窒化チタンなどのバリア導体膜２４ｂを約４５ｎｍ程度堆積し、バリア導体膜２４ａとバリア導体膜２４ｂとを合わせて、膜厚が約５０ｎｍ程度のバリア導体膜２４とする。そのバリア導体膜２４ｂの堆積には平行平板型マグネトロンスパッタリング装置、たとえばＡＭＡＴ社Ｅｎｄｕｒａ　ＨＰを用いたスパッタリング法を用い、その際の半導体基板１の温度は、バリア導体膜２４ａを堆積したときの半導体基板１の温度よりも高くてもよい（第２のスパッタリング工程）。

【００５８】その後、前記実施の形態１において図７および図８を用いて説明した工程と同様の工程にてプラグ２６を形成した後、半導体基板１の全面に、たとえば窒化チタンなどの導電性膜２７をスパッタリング法にて堆積する。この時、導電性膜２７の最初の５ｎｍ程度は、本実施の形態３においてバリア導体膜２４ａを堆積したときの条件と同じ条件にて堆積することで、チャージアップダメージによるゲート酸化膜９が破壊することを防ぐことができる。また、導電性膜２７のすべてをバリア導体膜２４ａを堆積したときの条件と同じ条件にて堆積してもよい。

【００５９】続いて、前記実施の形態１において図９および図１０を用いて説明した工程と同様の工程にて導電性膜２８および導電性膜２９を堆積し、パターニングすることで配線３０を形成する。

【００６０】続いて、前記実施の形態１において図１１を用いて説明した工程と同様の工程にて絶縁膜３１および接続孔３２を形成した後、本実施の形態３において説明したプラグ２６および配線３０の形成工程と同様の工程により、プラグ３３および配線３４を形成して、本実施の形態３の半導体集積回路装置を製造する。

【００６１】以上、本発明者によってなされた発明を発明の実施の形態に基づき具体的に説明したが、本発明は前記実施の形態に限定されるものではなく、その要旨を逸脱しない範囲で種々変更可能であることは言うまでもない。

【００６２】たとえば、実施の形態１において、チタン膜を用いてサリサイドを行いチタンシリサイド膜を形成したが、タングステン膜、モリブデン膜、タンタル膜またはコバルト膜を用いてシリサイド化反応を生じさせてもよい。

【００６３】

【発明の効果】本願によって開示される発明のうち、代表的なものによって得られる効果を簡単に説明すれば以下の通りである。

（１）本発明によれば、スパッタリング法にて薄膜を堆積する際に発生するプラズマ電子の半導体基板への流入を低減し、チャージアップダメージによるゲート酸化膜の破壊を防ぐことができる。

（２）本発明によれば、スパッタリング法にて薄膜を堆積する際のプラズマ電子のチャージアップによるゲート酸化膜の破壊を防止することができるので、半導体集積回路装置の歩留まりおよび信頼性を向上することができる。

【図面の簡単な説明】

【図１】本発明の一実施の形態である半導体集積回路装置の製造方法の一例を示した要部断面図である。

【図２】図１に続く半導体集積回路装置の製造工程中の要部断面図である。

【図３】コリメーションスパッタリング装置の説明図である。

【図４】ロングスロースパッタリング装置の説明図である。

【図５】スパッタリング装置のターゲットと半導体基板との間の距離と、ゲート酸化膜破壊（不良）率との関係を示す説明図である。

【図６】スパッタリング装置のターゲットと半導体基板

との間の距離と、プラズマ電子の流れを示す説明図である。

【図７】図２に続く半導体集積回路装置の製造工程中の要部断面図である。

【図８】図７に続く半導体集積回路装置の製造工程中の要部断面図である。

【図９】図８に続く半導体集積回路装置の製造工程中の要部断面図である。

【図１０】図９に続く半導体集積回路装置の製造工程中の要部断面図である。

【図１１】図１０に続く半導体集積回路装置の製造工程中の要部断面図である。

【図１２】本発明の他の実施の形態である半導体集積回路装置の製造方法の一例を示した要部断面図である。

【図１３】スパッタリング装置のアルゴンガスの圧力とゲート酸化膜破壊（不良）率との関係を示す説明図である。

【図１４】図１２に続く半導体集積回路装置の製造工程中の要部断面図である。

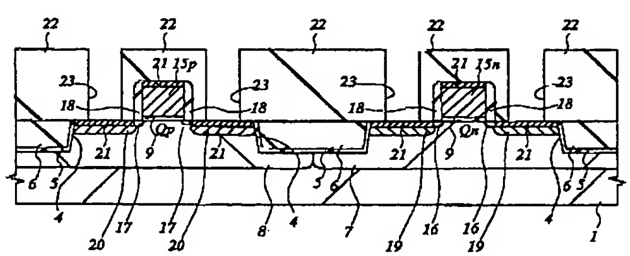
【図１５】半導体基板の温度とゲート酸化膜が破壊するときの電荷量との関係を示す説明図である。

【符号の説明】

１　半導体基板
４　素子分離溝
５　酸化シリコン膜
６　酸化シリコン膜
７　ｐ型ウェル
８　ｎ型ウエル
９　ゲート酸化膜
１５ｎ　ゲート電極
１５ｐ　ゲート電極
１６　ｎ⁻型半導体領域（ソース、ドレイン）
１７　ｐ⁻型半導体領域（ソース、ドレイン）
１８　サイドウォールスペーサ
１９　ｎ⁺型半導体領域（ソース、ドレイン）
２０　ｐ⁺型半導体領域（ソース、ドレイン）
２１　チタンシリサイド膜
２２　絶縁膜
２３　接続孔
２４　バリア導体膜（第１導電性膜）
２４ａ　バリア導体膜
２４ｂ　バリア導体膜
２５　導電性膜（第２導電性膜）
２６　プラグ
２７　導電性膜
２８　導電性膜
２９　導電性膜
３０　配線
３１　絶縁膜
３２　接続孔
３３　プラグ
３４　配線
Ｑｎ　ｎチャネル型ＭＩＳＦＥＴ
Ｑｐ　ｐチャネル型ＭＩＳＦＥＴ

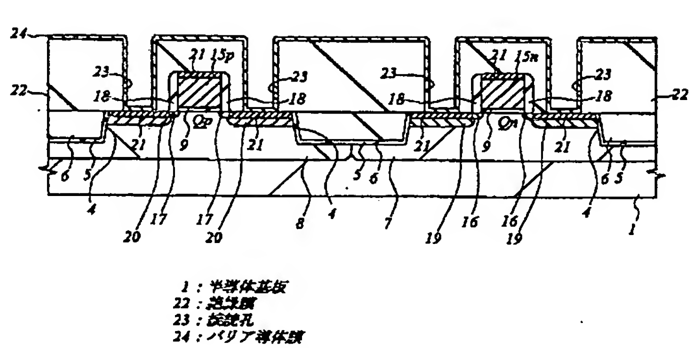
【図１】

図 1



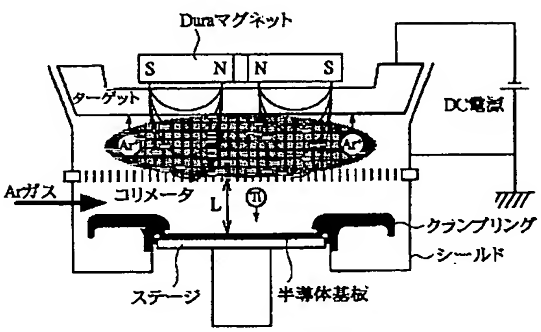
【図２】

図 2



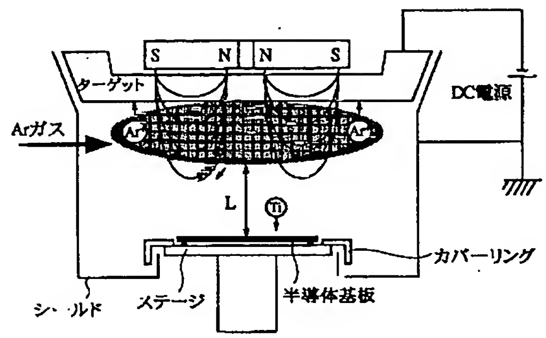
【図3】

図 3



【図4】

図 4



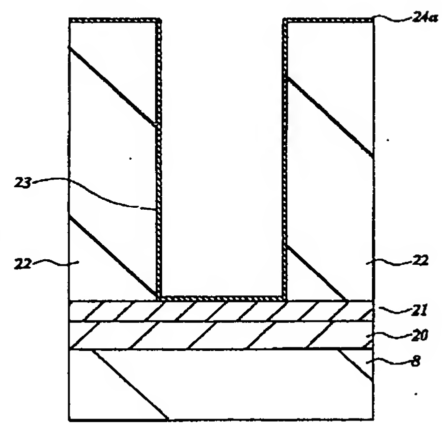
【図5】

図 5

ターゲット-半導体基板間距離	52mm（標準）	62mm
結果	[V] -6.89 -6.72 -6.74 -6.68 -6.74 -6.74 -6.71 -6.71 -6.68 -6.71 -6.71 -6.67 -6.63 -6.65 -6.66 -6.65 -6.67 -6.65 -6.67 -6.66 -6.60 -6.66 -6.64 -6.64 -6.65 -7.01 -6.63 -6.62 -6.64 -6.65 -7.15 -6.66 -6.70 -6.71	[V] -7.30 -7.35 -7.26 -7.31 -7.33 -7.33 -7.30 -7.29 -7.23 -7.27 -7.26 -7.27 -7.26 -7.29 -7.25 -7.23 -7.20 -7.10 -7.21 -7.19 -7.22 -7.21 -7.22 -7.21 -7.18 -7.16 -7.18 -7.22 -7.20 -7.10 -7.19 -7.17 -7.12 -7.12 -7.13 -7.16 -7.15 -7.16 -7.16 -7.19 -7.12 -7.00 -7.14 -7.15 -7.16 -7.16 -7.13
不良率	$\frac{22}{56}=39\%$	$\frac{9}{56}=16\%$

【図12】

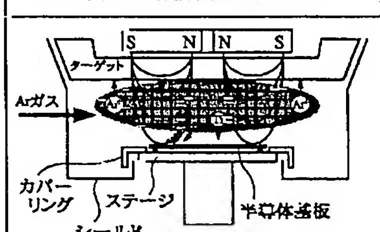
図 12



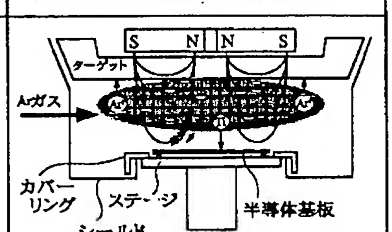
【図6】

図 6

ターゲット-半導体基板間距離＝52mm

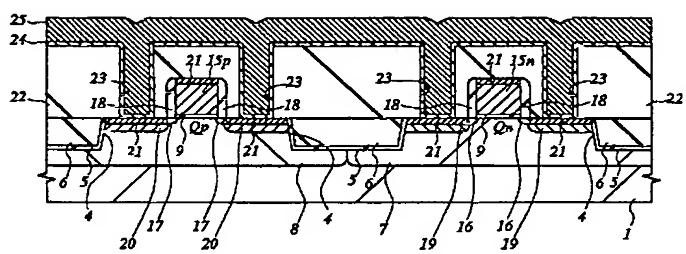


ターゲット-半導体基板間距離＝62mm



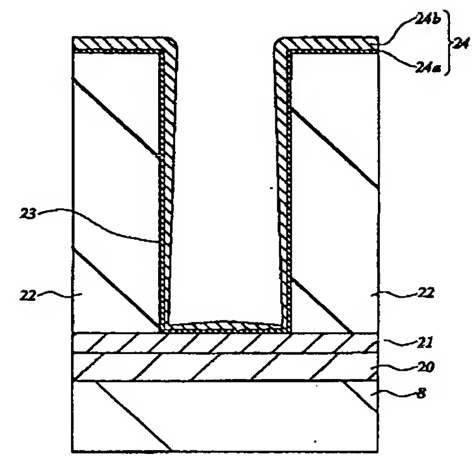
【図7】

図 7



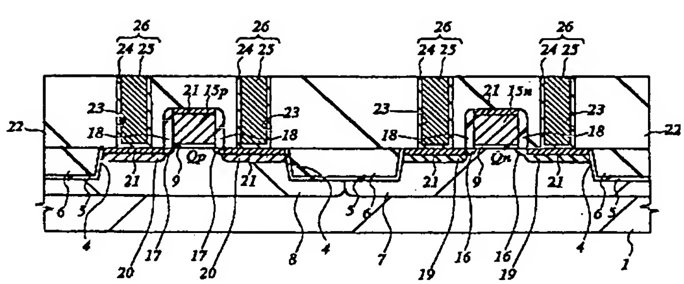
【図14】

図 14



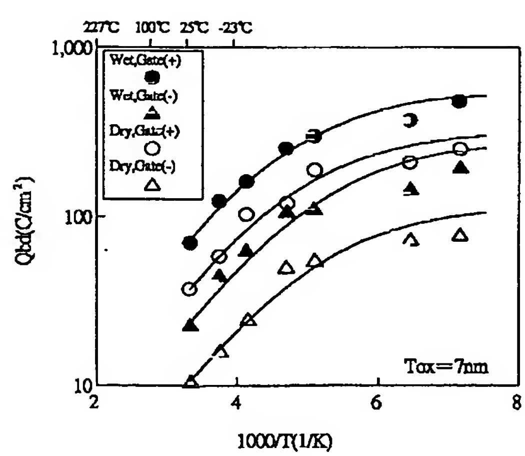
【図8】

図 8



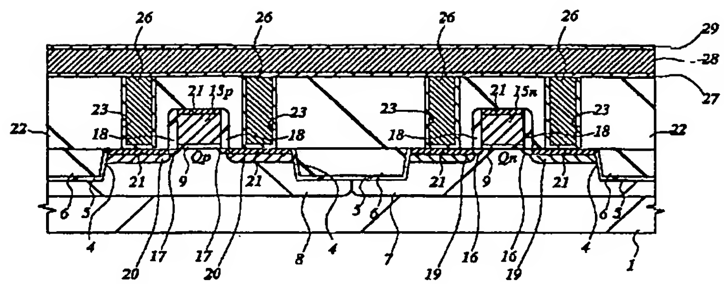
【図15】

図 15



【図9】

図 9



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21 15p
21 15n
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Qp
Qn
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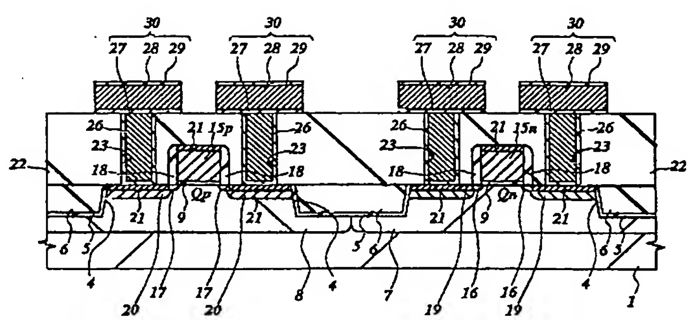
【図10】

図 10



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Qp
Qn
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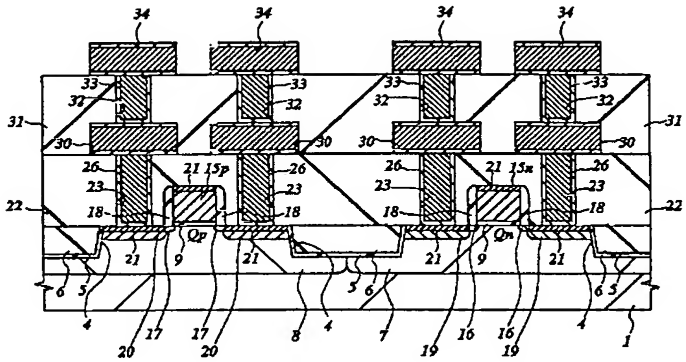
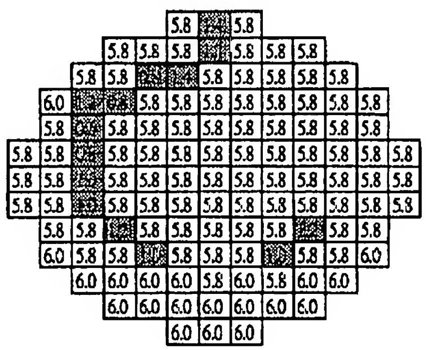
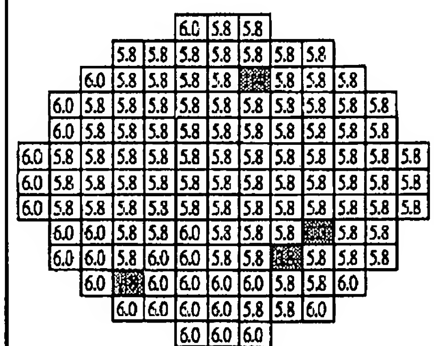
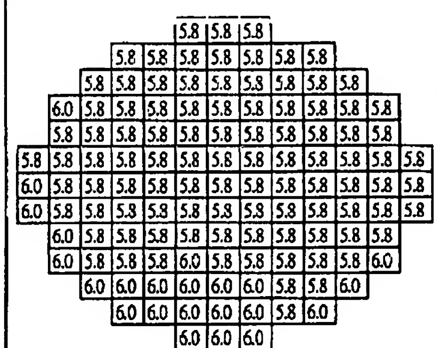
【図11】

図 11



【図13】

図 13

ガス圧力	2.0mTorr(≒0.266Pa)	3.5mTorr(≒0.4655Pa)	7.0mTorr(≒0.931Pa)
結果			
不良率	$\frac{14}{121}=11.6\%$	$\frac{4}{121}=3.6\%$	$\frac{0}{121}=0\%$

フロントページの続き

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DD75 DD78 DD84 EE03 FF16
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